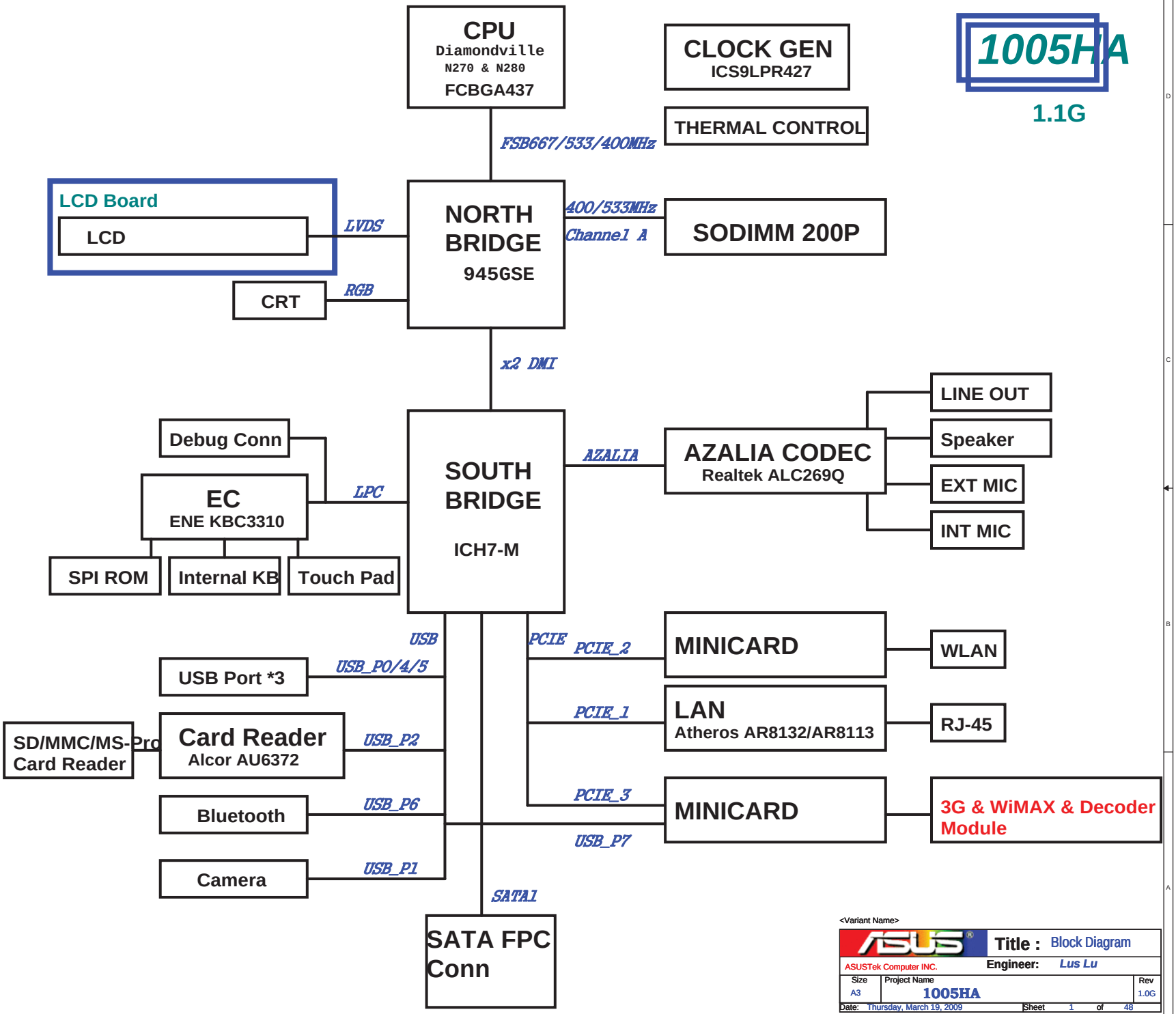


<Variant Name>

ASUSTek Computer INC.

Title : Block Diagram

Engineer: Lus Lu

Size	Project Name	Rev
A3	1005HA	1.0G

Date: Thursday, March 19, 2009 Sheet 1 of 48

EEE PC 701 PCB version

GPI37	GPI38	GPI39	PCB version
0	0	0	
0	0	0	
0	0	1	
0	0	1	
0	1	0	
0	1	0	
0	1	1	
0	1	1	
1	0	0	
1	0	0	
1	0	1	
1	0	1	
1	1	0	
1	1	0	
1	1	1	
1	1	1	

USB

USB 0	NC
USB 1	USB Conn
USB 2	USB Conn
USB 3	USB Conn
USB 4	Card Reader
USB 5	Minicard
USB 6	Bluetooth
USB 7	Camera

PCIE

PCIE 1	NC
PCIE 2	LAN
PCIE 3	Minicard
PCIE 4	SSD

Azalia

ACZ_SDIN0	CODEC
ACZ_SDIN1	NC
ACZ_SDIN2	NC

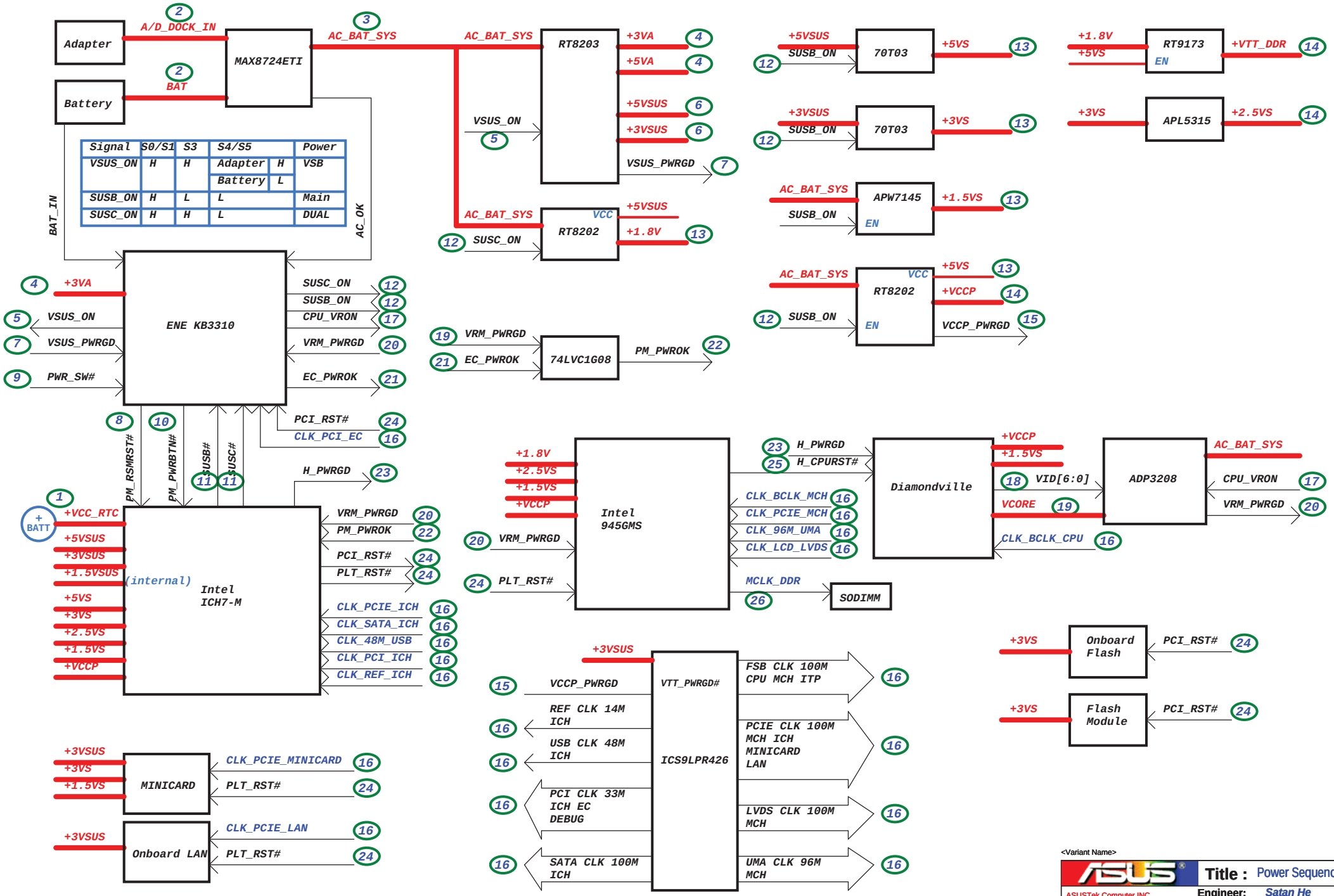
<Variant Name>

Title : System Setting

ASUSTek Computer INC. Engineer: Satan_He

Size	Project Name	Rev
A3	1005HA	1.0G

Date: Thursday, March 19, 2009 Sheet 2 of 48



<Variant Name>

ASUSTek Computer INC.

Title : Power Sequence

Engineer: Satan He

Size	Project Name	Rev
A3	S101	1.0G

Date: Thursday, March 19, 2009 Sheet 3 of 48

0.1B Beta

1:Disable
0:Enable

PEREQ1:PCIEx0 & PCIEx1
PEREQ2:PCIEx2 & PCIEx3 & SATA
PEREQ3:PCIEx4 & PCIEx5 & PCIEx6

If the PCICLK is driving two devices (2 loads),the series resisters need to be changed. (12 Ohm or 22 Ohm is recommended.)

CU1 ICS9LPRS427CGLFT

O_DOC1	O_DOC2	Voltage	Status
L	L	2.0-3.3V	Super
L	H	0.7-1.5V	Normal
H	*	0V	Power saving

FSLC	FSLB	FSLA	CPU(MHZ)
0	0	1	133.33
0	1	1	166

CLK_FSLC	Straping Define
1.8V-3.3V	enter Test Mode
0.7V-1.8V	FSB trap High
0V-0.35V	FSB trap Low

<Variant Name>

ASUSTek Computer INC.

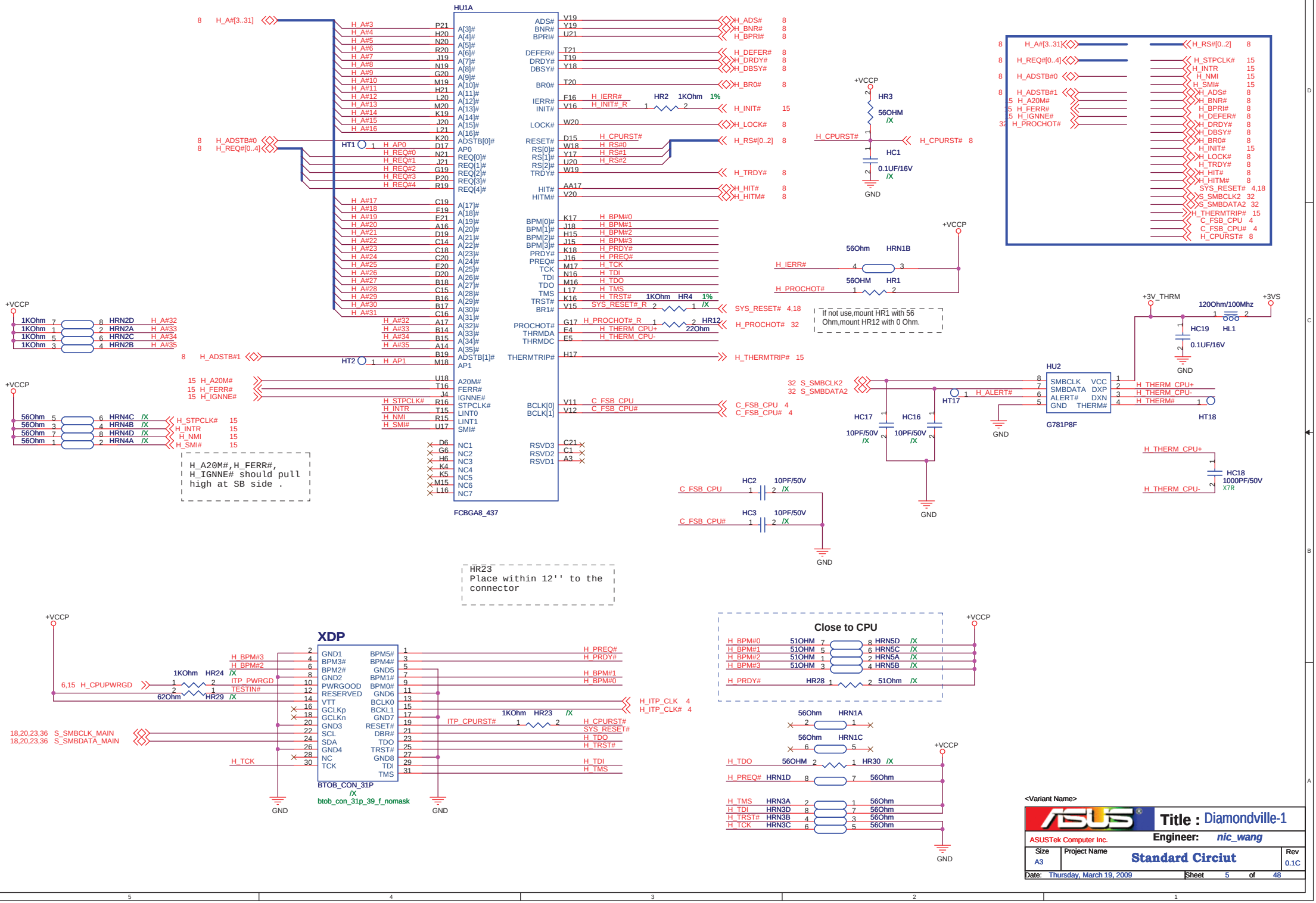
Title : Clock Gen_ICS9LPR427

Engineer: nic_wang

Size	Project Name	Rev
A3	standard circiut	0.1B

Date: Thursday, March 19, 2009 Sheet 4 of 48

0.1C Beta

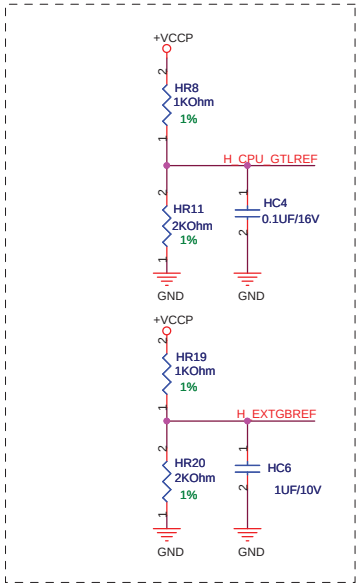


<variant_name>

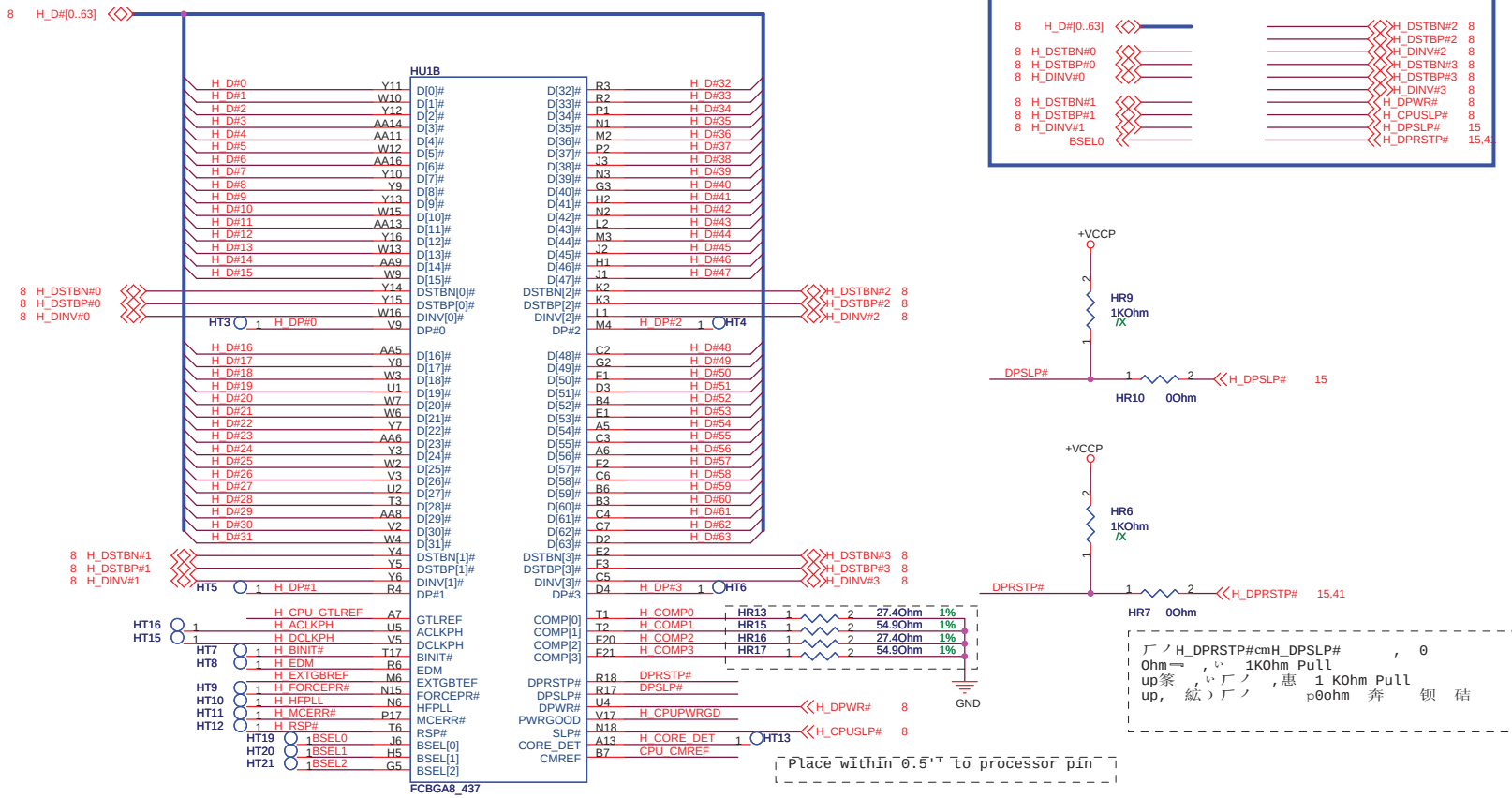
ASUSTek Computer Inc.	Title : Diamondville-1	
	Engineer: nic_wang	
Size: A3	Project Name: Standard Circiut	Rev: 0.1C
Date: Thursday, March 19, 2009	Sheet 5 of 48	

0.1C Beta

Place within 0.5'' to processor pin

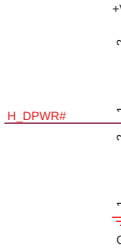


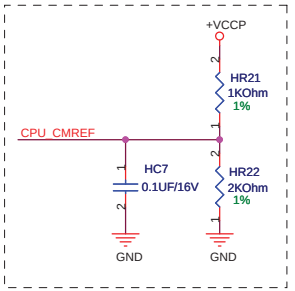
BSEL0	BSEL1	BSEL2	FSB
0	X	X	400
1	X	X	533



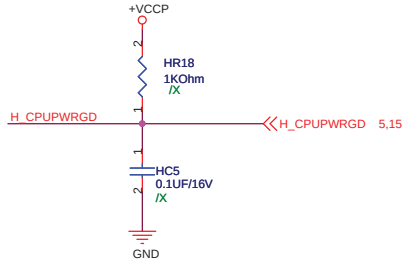
Place within 0.5'' to processor pin

厂ノH_DPRSTP#cmH_DPSLP# , 0
Ohm⇒ ,い 1KOhm Pull
up篆 ,い厂ノ ,惠 1 KOhm Pull
up, 紜 》厂ノ p0ohm 奔 钡 砧





Place within 0.5'' to processor pin



H_PWRGD-->H_CPUPWRGD

<Variant Name>

Title : Diamondville-2

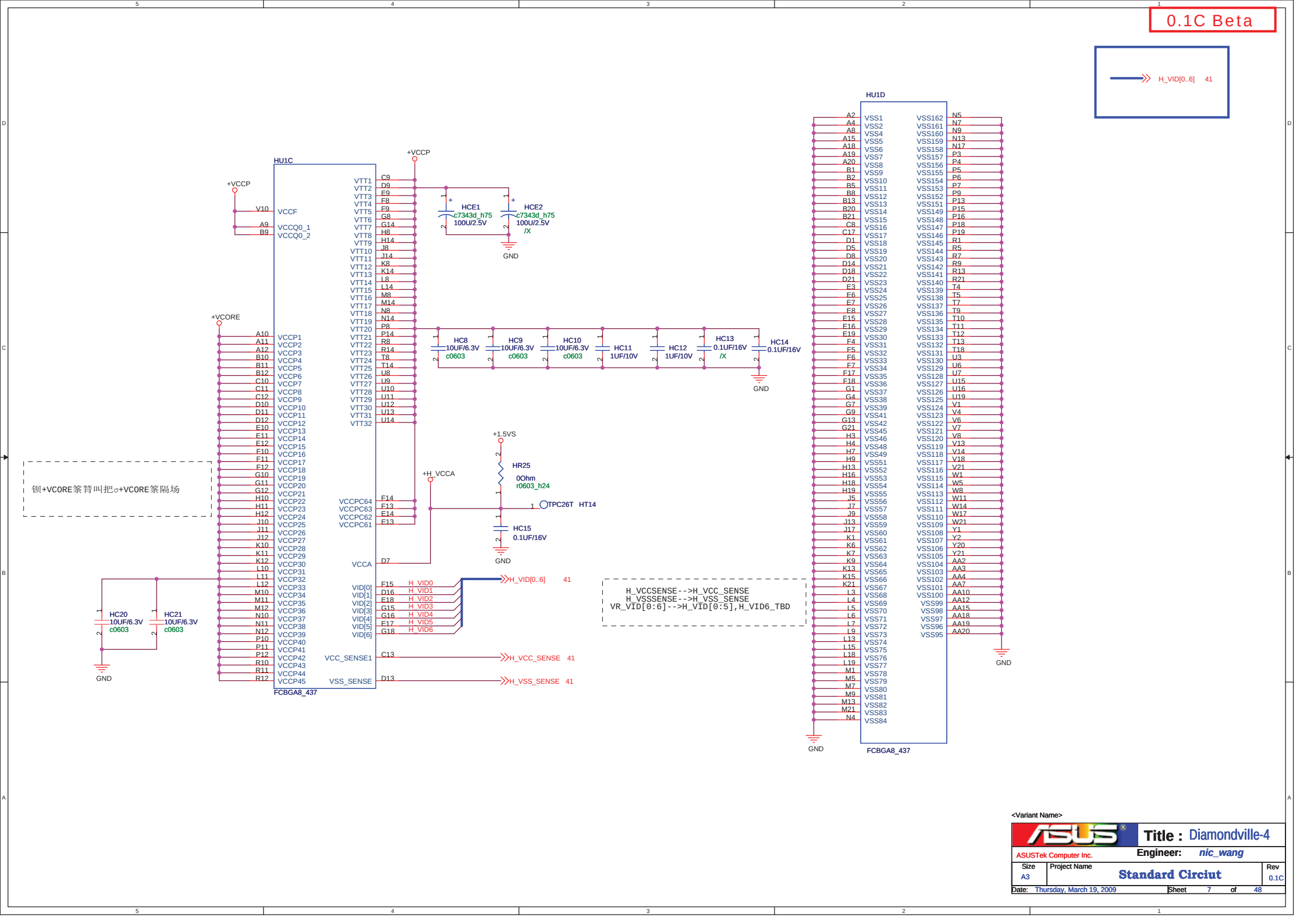
ASUSTek Computer Inc.

Engineer: nic_wang

Size	Project Name	Rev
A3	Standard Circiut	0.1C

Date: Thursday, March 19, 2009 Sheet 6 of 48

0.1C Beta



<Variant Name>

Title : Diamondville-4

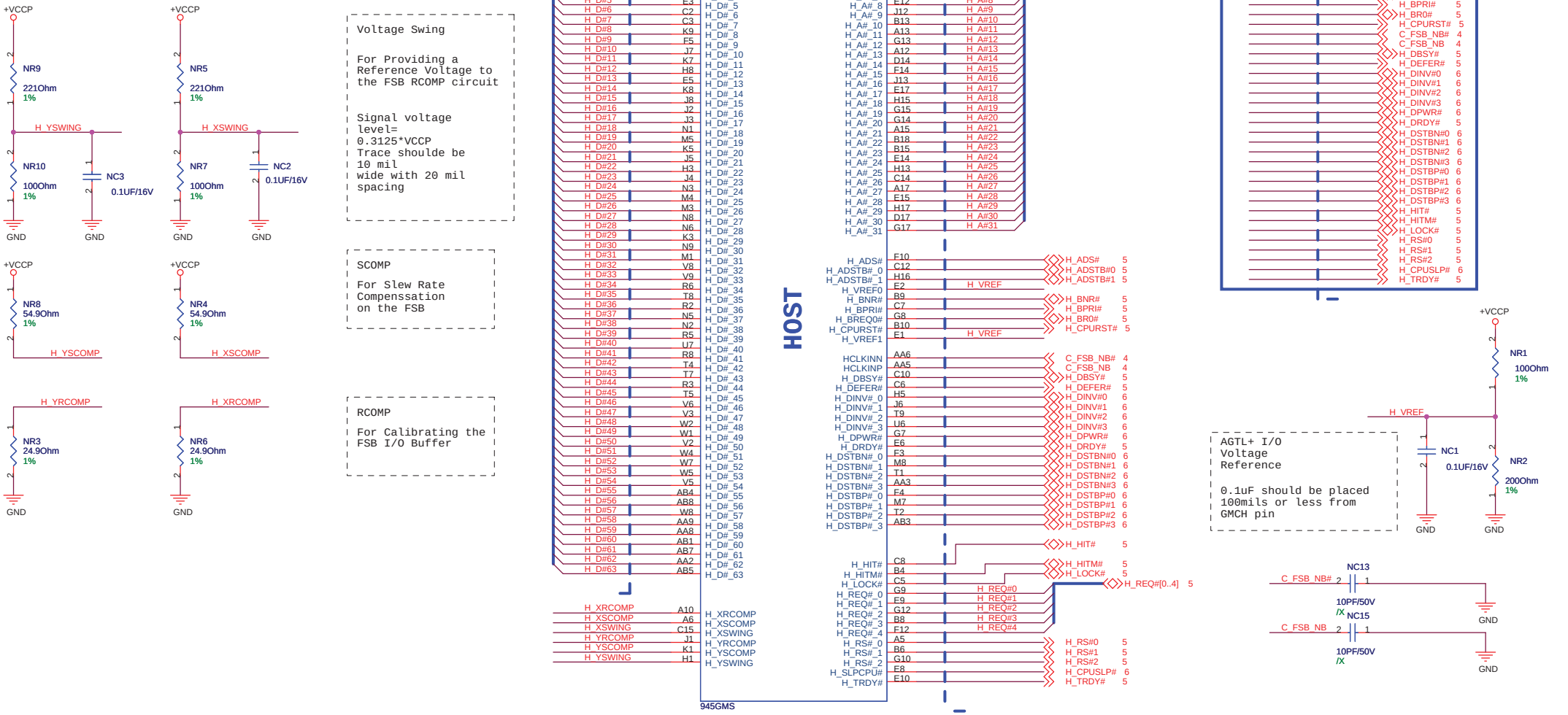
ASUSTek Computer Inc.

Engineer: nic_wang

Size	Project Name	Rev
A3	Standard Circiut	0.1C

Date: Thursday, March 19, 2009 Sheet 7 of 48

0.1D Beta



<Variant Name>

ASUSTeK COMPUTER INC.	Title : 945GSE-1(HOST)	
	Engineer: greenstar_xiao	
Size: A3	Project Name: Standard Circuit	Rev: 0.1D
Date: Thursday, March 19, 2009	Sheet 8 of 48	

0.1D Beta

BCLK	FSB	BSEL2	BSEL1	BSEL0
133	533	L	L	H
166	667	L	H	H

+VCCP +VCCP

NR11 1KOhm N/A

NR12 1KOhm

NR14 0Ohm /X

GND GND

N_BSEL0 N_BSEL1 N_BSEL2 DMIX2_SELECT

CFG_3 & CFG_6
Reserved

NU1B

CFG_0 CFG_1 CFG_2 CFG_3 CFG_5 CFG_6

RESERVED1 RESERVED2 RESERVED7 RESERVED8 RESERVED9

CFG/RSVD

DMI_RXN_0 DMI_RXN_1 DMI_RXP_0 DMI_RXP_1

DMI_TXN_0 DMI_TXN_1 DMI_TXP_0 DMI_TXP_1

DMI

DMI_RXN0 17
DMI_RXN1 17
DMI_RXP0 17
DMI_RXP1 17

DMI_TXN0 17
DMI_TXN1 17
DMI_TXP0 17
DMI_TXP1 17

SM_CK_0 SM_CK_1 SM_CK_2 SM_CK_3

SM_CK#_0 SM_CK#_1 SM_CK#_2 SM_CK#_3

SM_CKE_0 SM_CKE_1 SM_CKE_2 SM_CKE_3

SM_CS#_0 SM_CS#_1 SM_CS#_2 SM_CS#_3

SM_ODT_0 SM_ODT_1 SM_ODT_2 SM_ODT_3

SM_RCOMPN SM_RCOMPP SM_VREF_0 SM_VREF_1

DDR2 MUXING

D2_MA_CLK0 20
D2_MA_CLK1 20

D2_MA_CLK#0 20
D2_MA_CLK#1 20

D2_CKE_A0 20,21
D2_CKE_A1 20,21

D2_CS_A#0 20,21
D2_CS_A#1 20,21

D2_ODT_A0 20,21
D2_ODT_A1 20,21

DMIX2_SELECT

0=DMI X2(DEFAULT)
1=Reserved

NR15 2.7KOHM

GND

A 10K-Ω pull up resistor has been used on the PM_EXTTS#_1, if the Fast C4E feature is required, this resistor has to be unstuffed.

+3VS

10KOhm NR38 NR39 10KOhm /X

16 ICH_SYNC#
18 PM_BMBUSY#

ICH_SYNC# PM_BMBUSY# PM_EXTTS#_0 PM_EXTTS#_1 THRMTRIP# PWROK RSTIN#

PM

N_PM_EXTTS#0 N_PM_EXTTS#1 THERMTRIP#

NT1

18,32 PM_PWROK
16,18 SPLTRST#

N_PLTRST#

NR22 100Ohm 1%

4 C_96M_NB#
4 C_96M_NB
4 C_LCD_LVDS#
4 C_LCD_LVDS
4 C_REQ#_NB

D_REFCLKINN D_REFCLKINP D_REFSSCLKINN D_REFSSCLKINP CLKREQ#

CLK

NR100 0Ohm /X

945GMS

AJ21 N_OCDCOMP_0
AF11 N_OCDCOMP_1

NR18 40.2Ohm /X 1%

NR19 40.2Ohm /X 1%

GND

AE12 D2_ODT_A0 20,21
AE14 D2_ODT_A1 20,21

+1.8V

AN12 N_RCOMPN
AN14 N_RCOMPP

NR23 80.6Ohm 1%

NR24 80.6Ohm 1%

GND

AA33 AE1 N_VREF_MCH

+1.8V

NR25 1KOhm 1%

N_VREF_MCH

Place NC27 close to AA33 Pin

Place NC4 close to AE1 Pin

NC27 0.1UF/16V

NC4 0.1UF/16V

NR28 1KOhm 1%

GND GND GND

N_PM_EXTTS#1 NR37 0Ohm PM_DPRSLPVR 18,41

0.1C Bate

EXTTS1# can alternately be used to implement fast C4/C4E exit,IF the Fast C4E feature is required,PM_EXTTS1# have to connect to DPRSLPVR

C_96M_NB# NC67 10PF/50V /X GND

C_96M_NB NC68 10PF/50V /X GND

C_LCD_LVDS# NC69 10PF/50V /X GND

C_LCD_LVDS NC70 10PF/50V /X GND

DMI_RXN0 17
DMI_RXN1 17
DMI_RXP0 17
DMI_RXP1 17

DMI_TXN0 17
DMI_TXN1 17
DMI_TXP0 17
DMI_TXP1 17

D2_MA_CLK0 20
D2_MA_CLK1 20
D2_MA_CLK#0 20
D2_MA_CLK#1 20
D2_CKE_A0 20,21
D2_CKE_A1 20,21
D2_CS_A#0 20,21
D2_CS_A#1 20,21
D2_ODT_A0 20,21
D2_ODT_A1 20,21

ICH_SYNC# 16
PM_BMBUSY# 18
PM_PWROK 18,32
SPLTRST# 16,18
C_96M_NB# 4
C_96M_NB 4
C_LCD_LVDS# 4
C_LCD_LVDS 4
C_REQ#_NB 4
PM_DPRSLPVR 18,41

<Variant Name>

ASUSTek Computer Inc.

Title : 945GSE-2(DMI&CFG)

Engineer: greenstar_xiao

Size	Project Name	Rev
A3	Standard Circuit	0.1D

Date: Thursday, March 19, 2009 Sheet 9 of 48

0.1D Beta

NR29
NR30
NR32
Close to GMCH

NC33 10PF/50V /X
NC36 10PF/50V /X

NU1F

945GMS

NR31 24.9Ohm 1%
Place NR31 within 500mils of GMCH
Avoid rounting next to clock pins

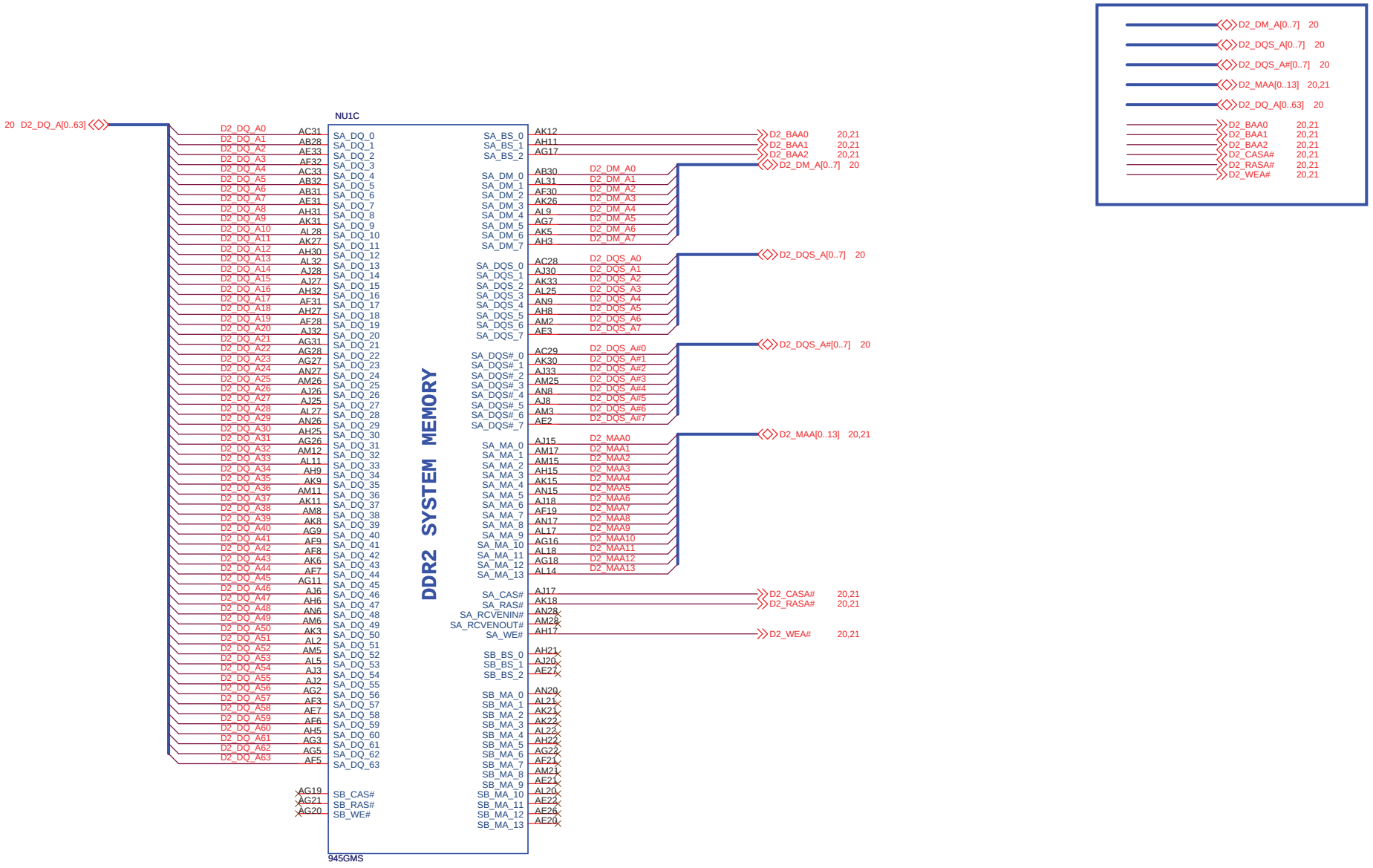
NR33,NR34 decide by EA test

For Disable TV

<Variant Name>

ASUSTek Computer Inc.	Title : 945GSE-3(GRAPHIC)	
	Engineer: greenstar_xiao	
Size: A3	Project Name: Standard Circuit	Rev: 0.1D
Date: Thursday, March 19, 2009	Sheet 10 of 48	

0.1D Beta



<Variant Name>

ASUSTek Computer Inc.

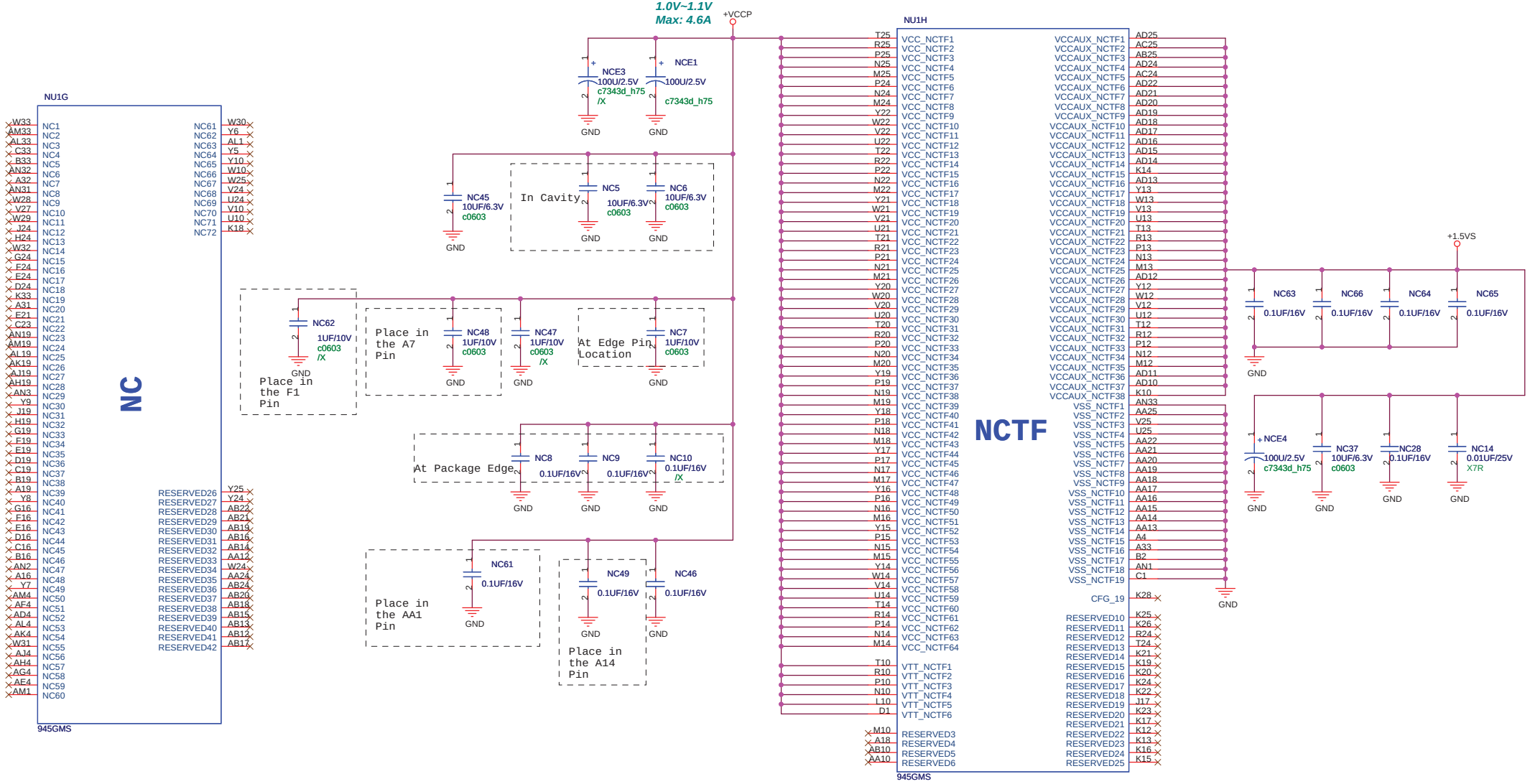
Title : 945GSE-4(DDR2)

Engineer: greenstar_xiao

Size	Project Name	Rev
A3	Standard Circuit	0.1D

Date: Thursday, March 19, 2009 Sheet 11 of 48

0.1D Beta



<Variant Name>

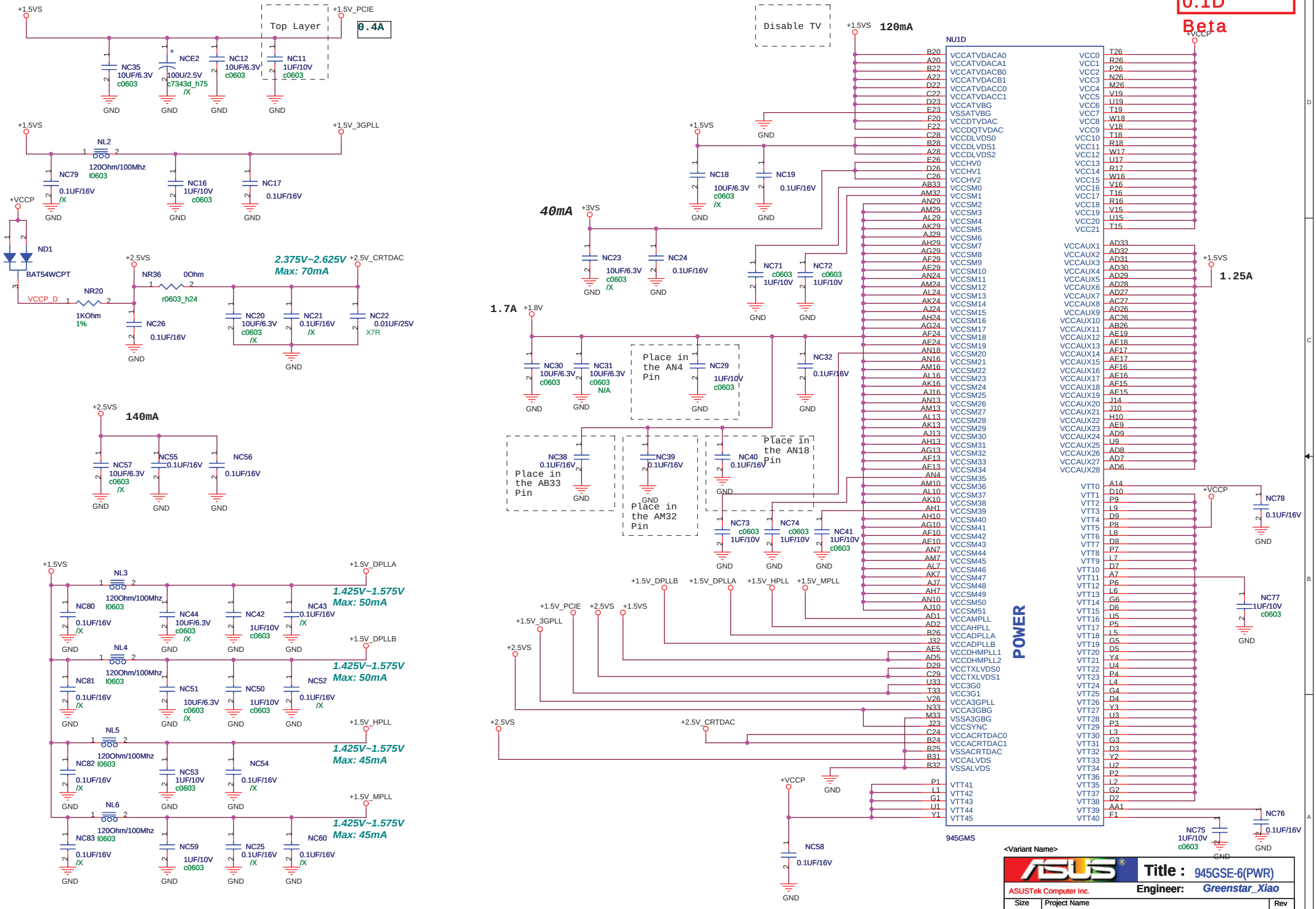
ASUSTek Computer Inc.

Title : 945GSE-5(NC&NCTF)

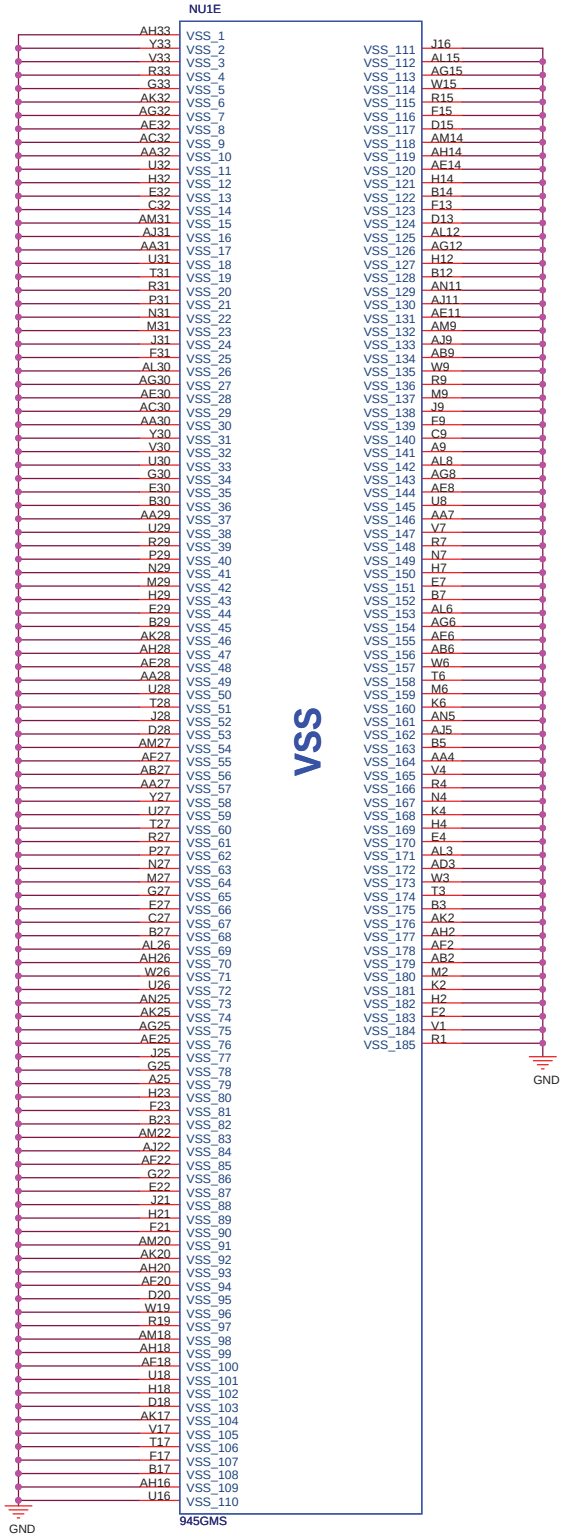
Engineer: greenstar_xiao

Size	Project Name	Rev
A3	Standard Circuit	0.1D

Date: Thursday, March 19, 2009 Sheet 12 of 48


0.1D
Beta
Top Layer
0.4A
Disable TV
120mA
1.25A
40mA
1.7A
140mA
2.375V~2.625V
Max: 70mA
1.425V~1.575V
Max: 50mA
1.425V~1.575V
Max: 50mA
1.425V~1.575V
Max: 45mA
1.425V~1.575V
Max: 45mA
Place in the AN4 Pin
Place in the AN18 Pin
Place in the AB33 Pin
Place in the AM32 Pin
NU1D
945GMS
POWER
<Variant Name>
Title : 945GSE-6(PWR)
ASUSTek Computer Inc.
Engineer: Greenstar_Xiao
Size A3
Project Name Standard Circuit
Rev 0.1D
Date: Thursday, March 19, 2009
Sheet 13 of 48

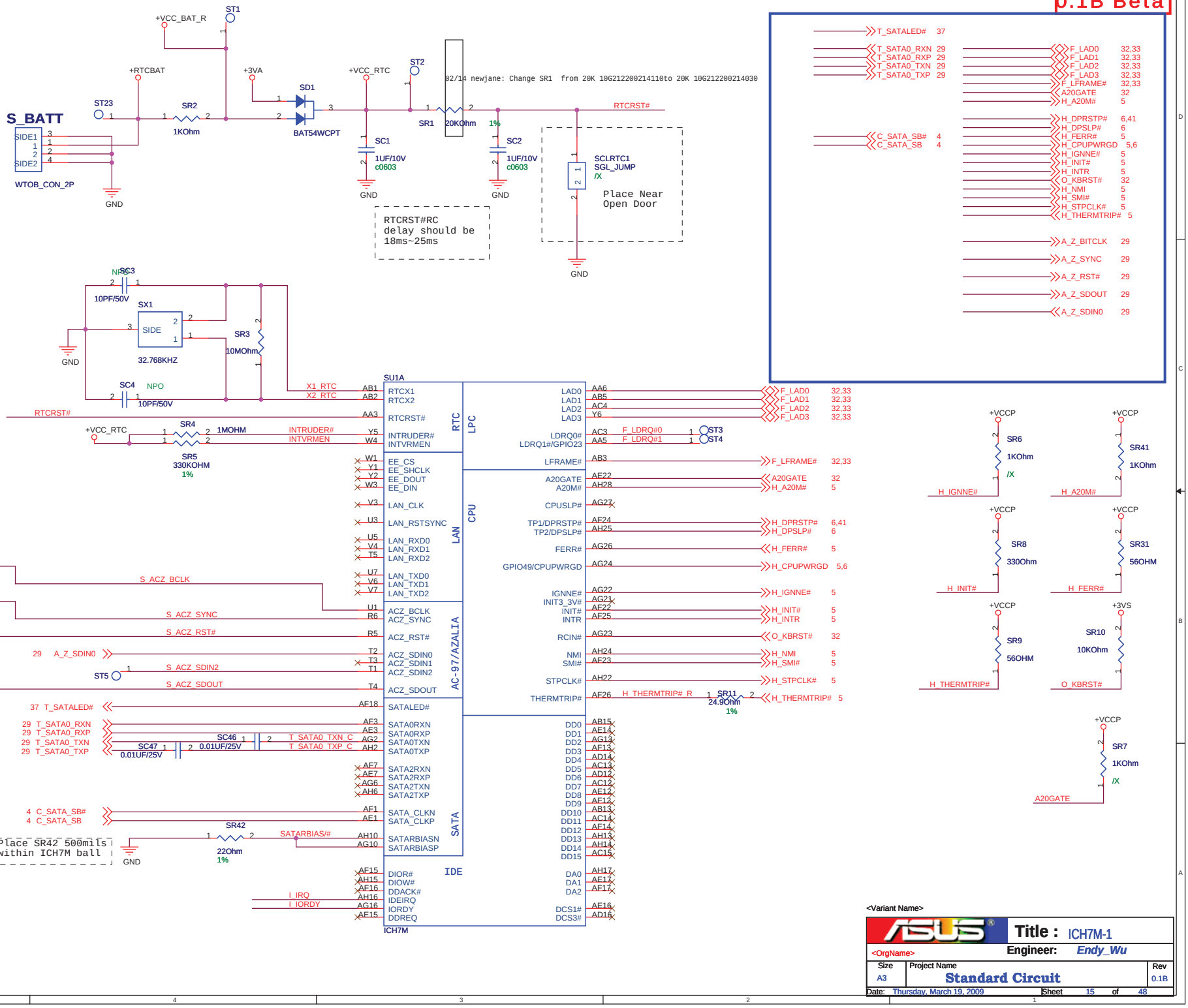
0.1D Beta



<Variant Name>

ASUSTek Computer Inc.	Title : 945GSE-7(GND)	
	Engineer: Greenstar_Xiao	
Size: A3	Project Name: Standard Circuit	Rev: 0.1D
Date: Thursday, March 19, 2009	Sheet 14 of 48	

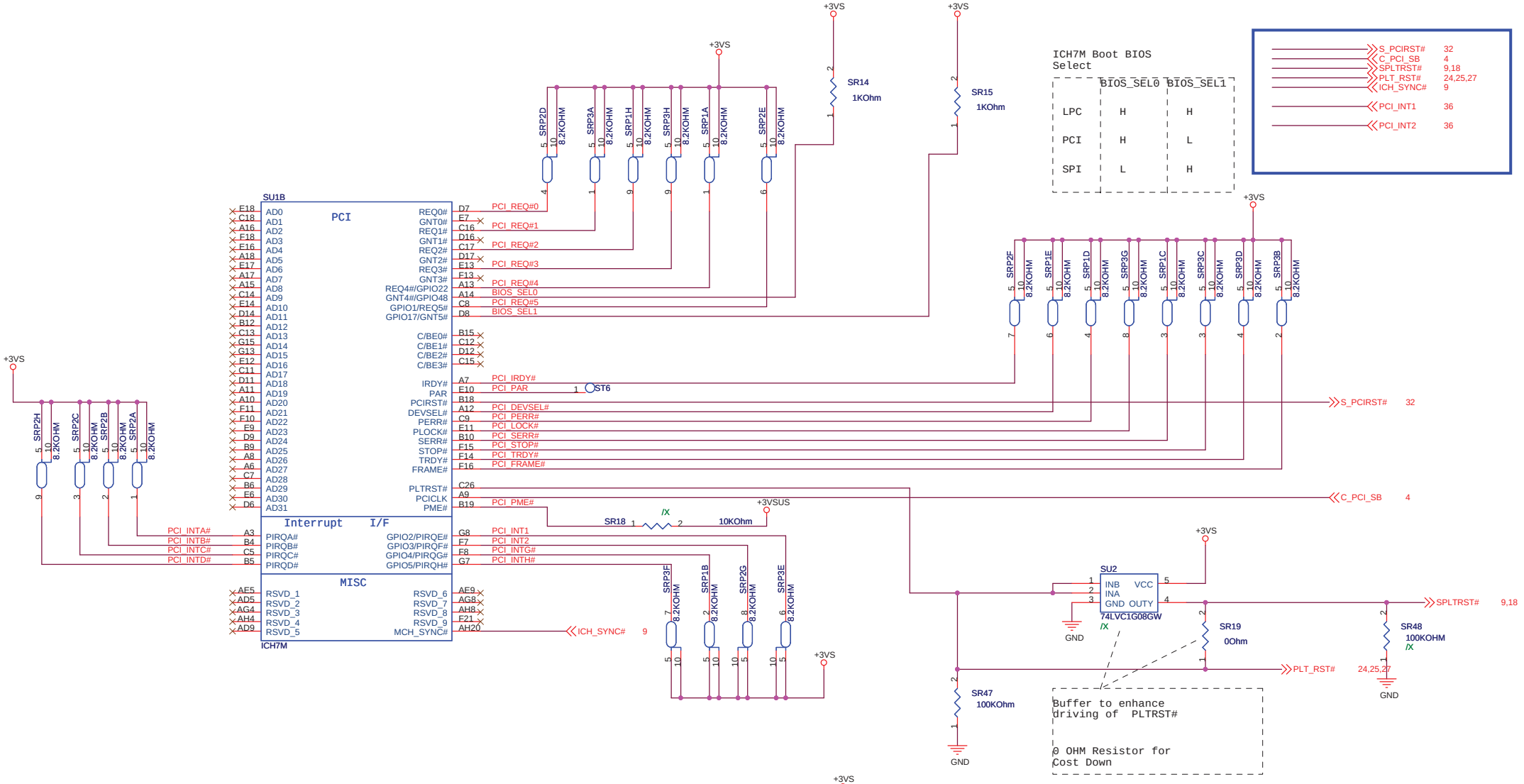
0.1B Beta



<Variant Name>

<OrgName>	Title : ICH7M-1	
	Engineer: Endy_Wu	
Size: A3	Project Name: Standard Circuit	Rev: 0.1B
Date: Thursday, March 19, 2009	Sheet 15 of 48	

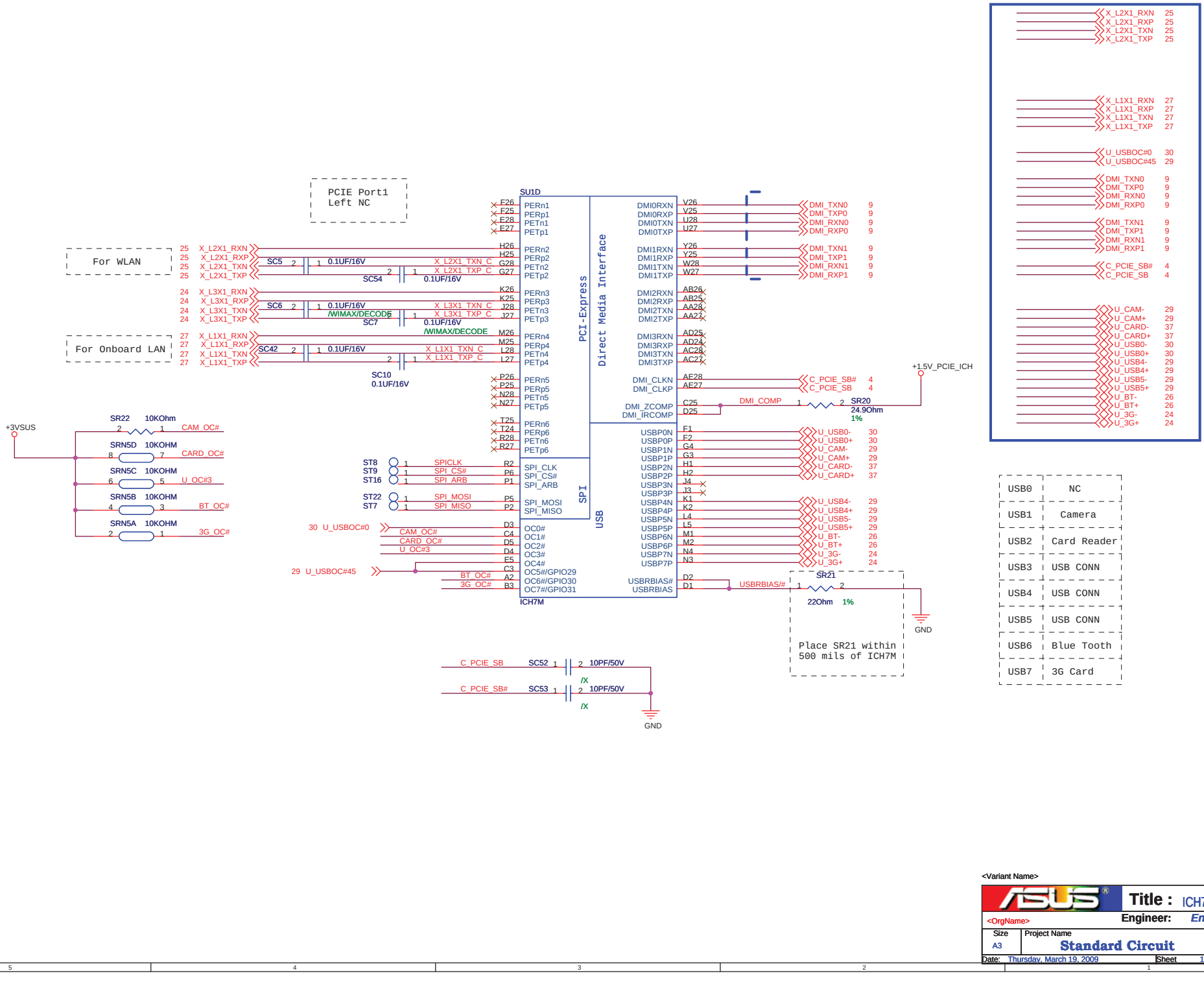
0.1B Beta



<Variant Name>

<OrgName>	Title : ICH7M-2	
	Engineer: Endy_Wu	
Size: A3	Project Name: Standard Circuit	Rev: 0.1B
Date: Thursday, March 19, 2009	Sheet 16 of 48	

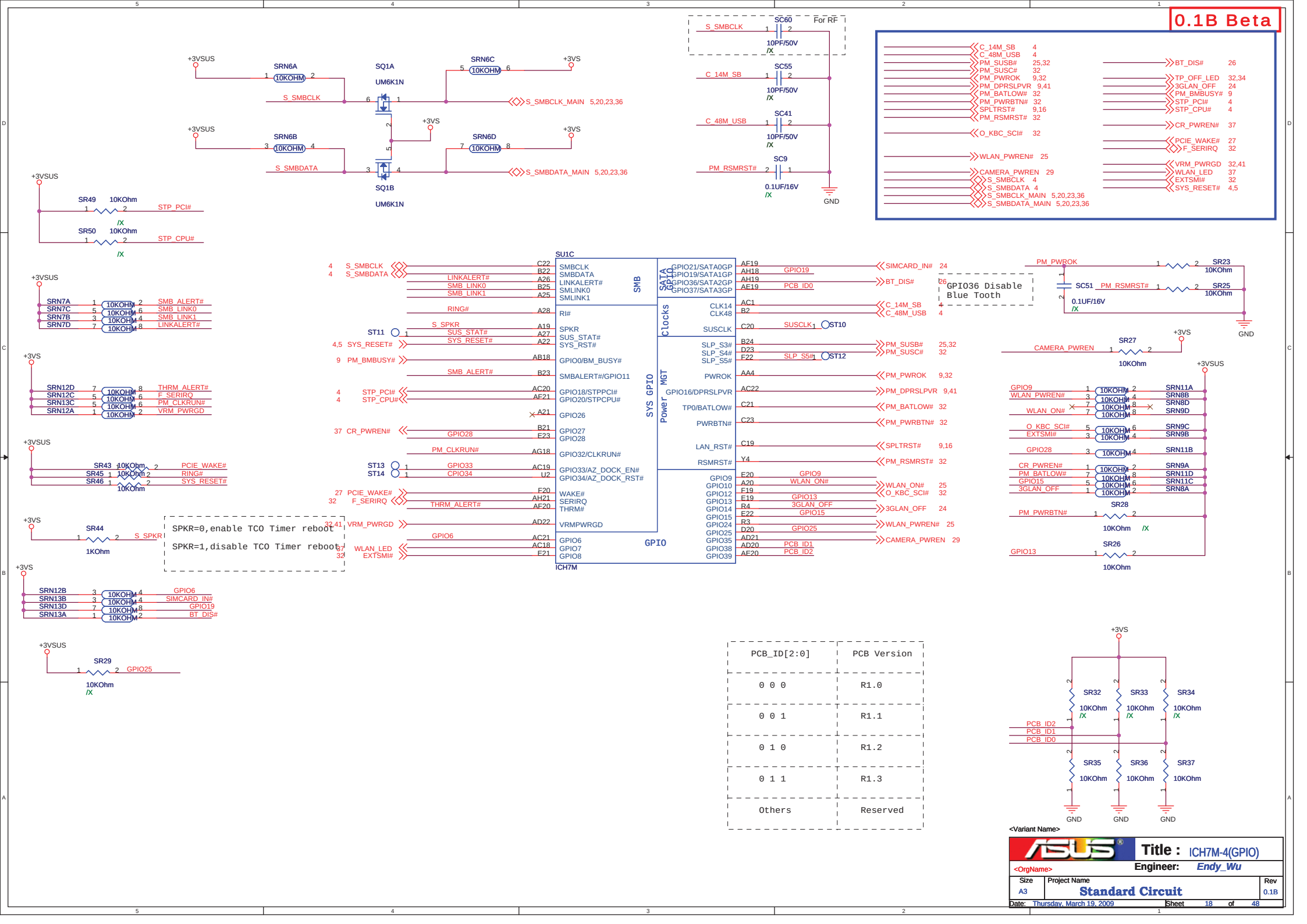
0.1B Beta



<Variant Name>

<OrgName>	Title : ICH7M-3	
	Engineer: Endy_Wu	
Size: A3	Project Name: Standard Circuit	Rev: 0.1B
Date: Thursday, March 19, 2009	Sheet 17 of 48	

0.1B Beta



<Variant Name>

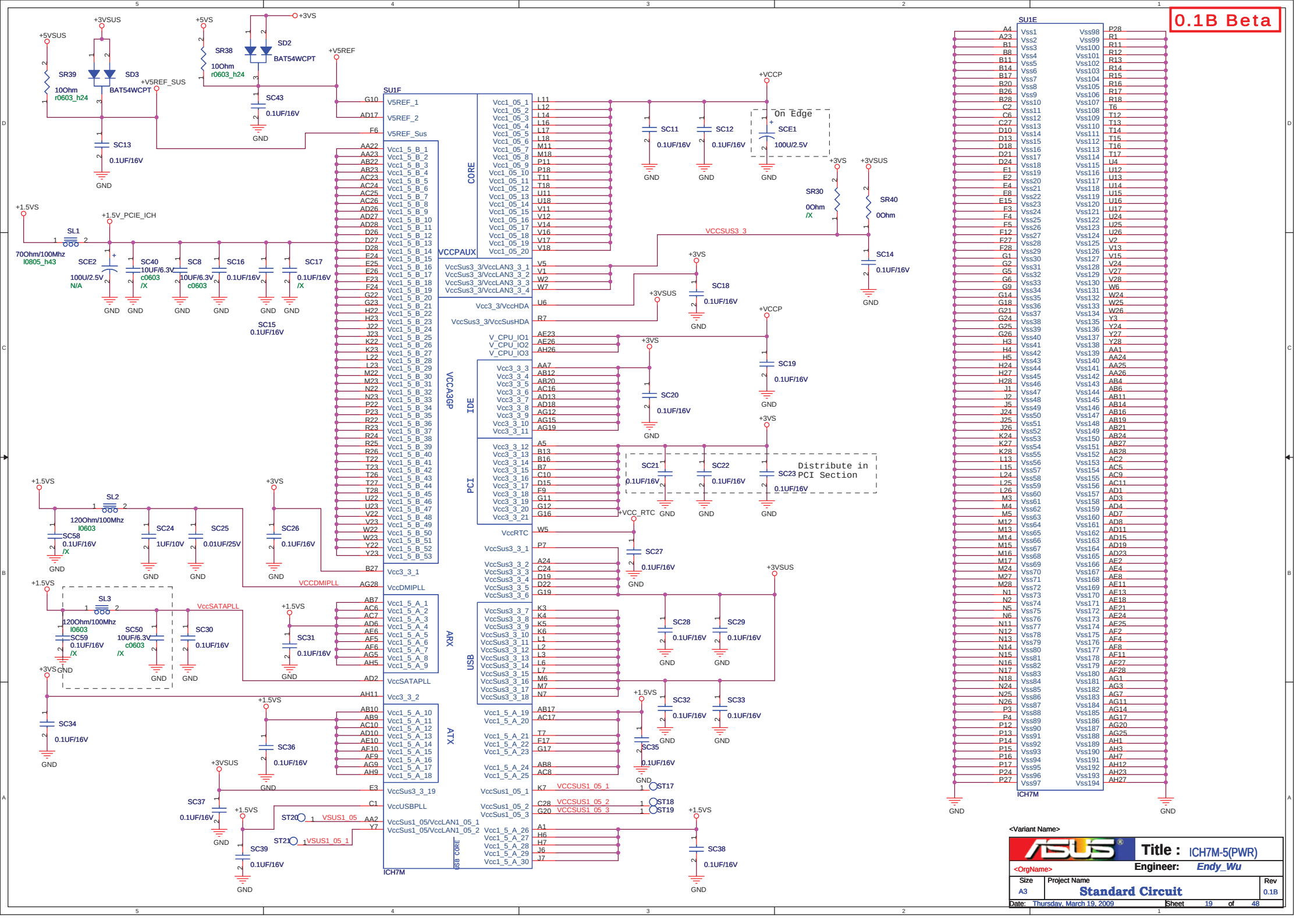
ASUS

Title : ICH7M-4(GPIO)

<OrgName> Engineer: Endy_Wu

Size	Project Name	Rev
A3	Standard Circuit	0.1B

Date: Thursday, March 19, 2009 Sheet 18 of 48



<Variant Name>

ASUS

Title : ICH7M-5(PWR)

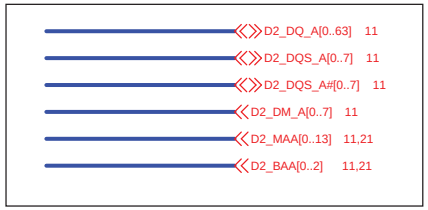
<OrgName>

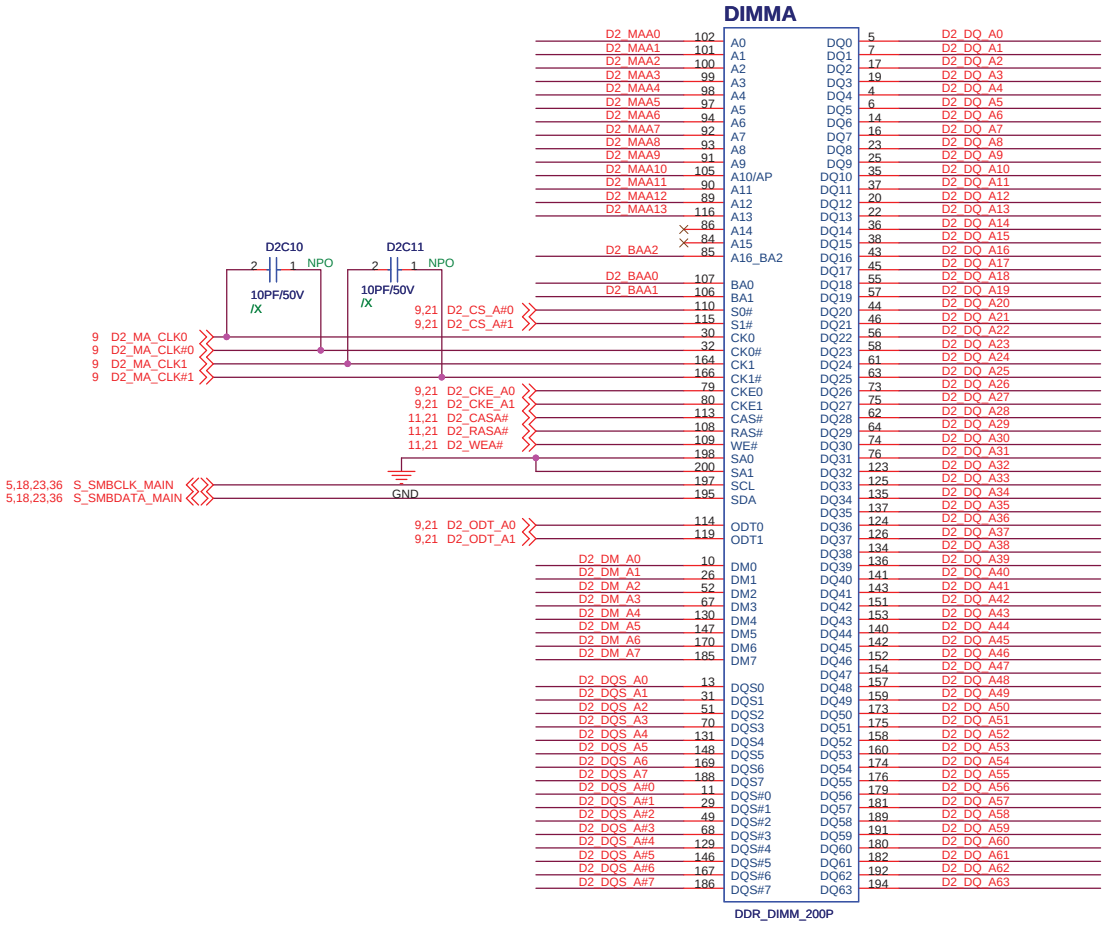
Engineer: Endy_Wu

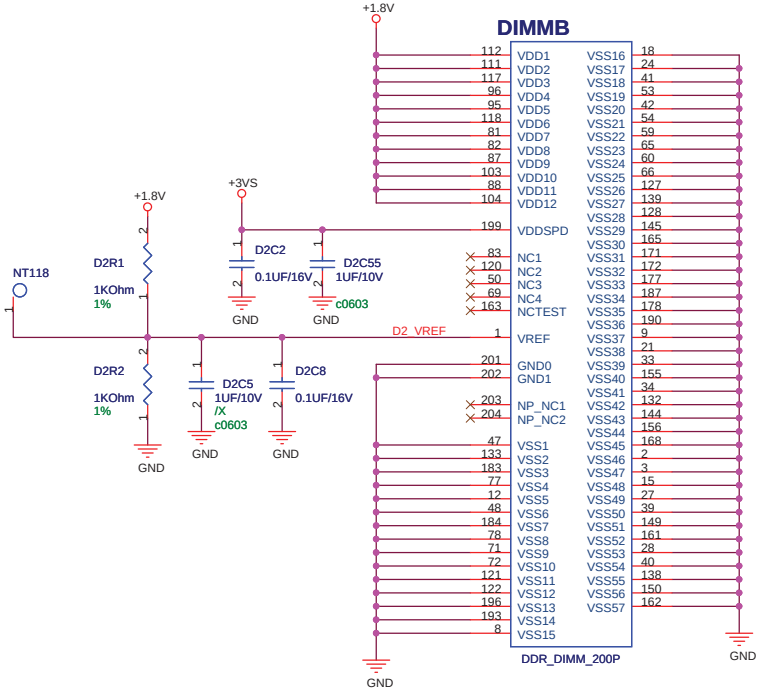
Size	Project Name	Rev
A3	Standard Circuit	0.1B

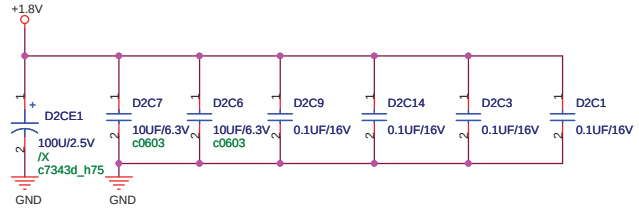
Date: Thursday, March 19, 2009 Sheet 19 of 48

0.1B Beta





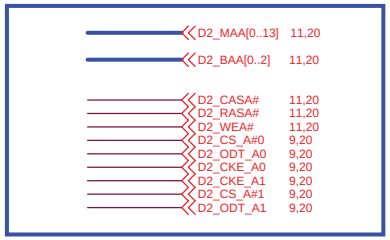


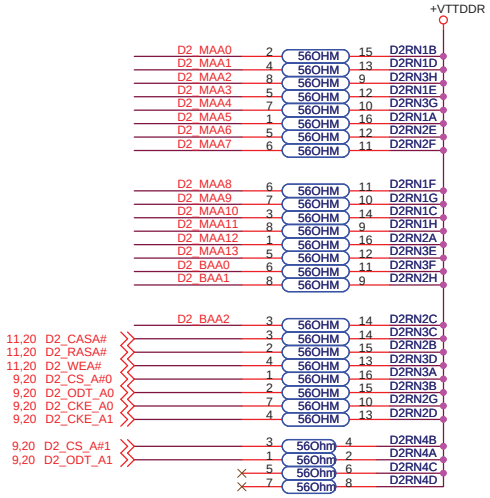


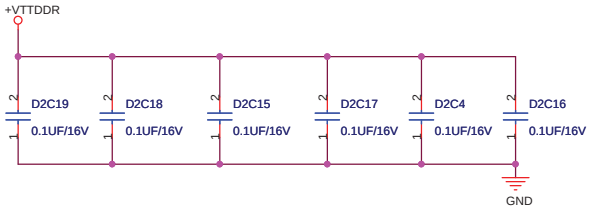
<variant_name>

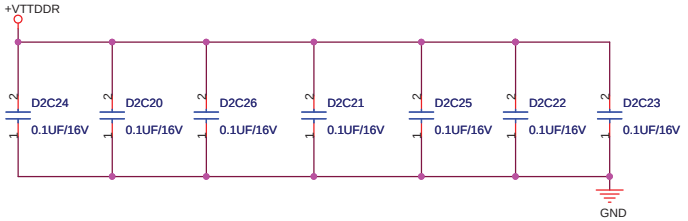
ASUSTek Computer INC.	Title : DDR2-SO-DIMM	
	Engineer: Endy_Wu	
Size: A3	Project Name: Standard Circuit	Rev: 0.1B
Date: Thursday, March 19, 2009	Sheet 20 of 48	

0.1B Beta





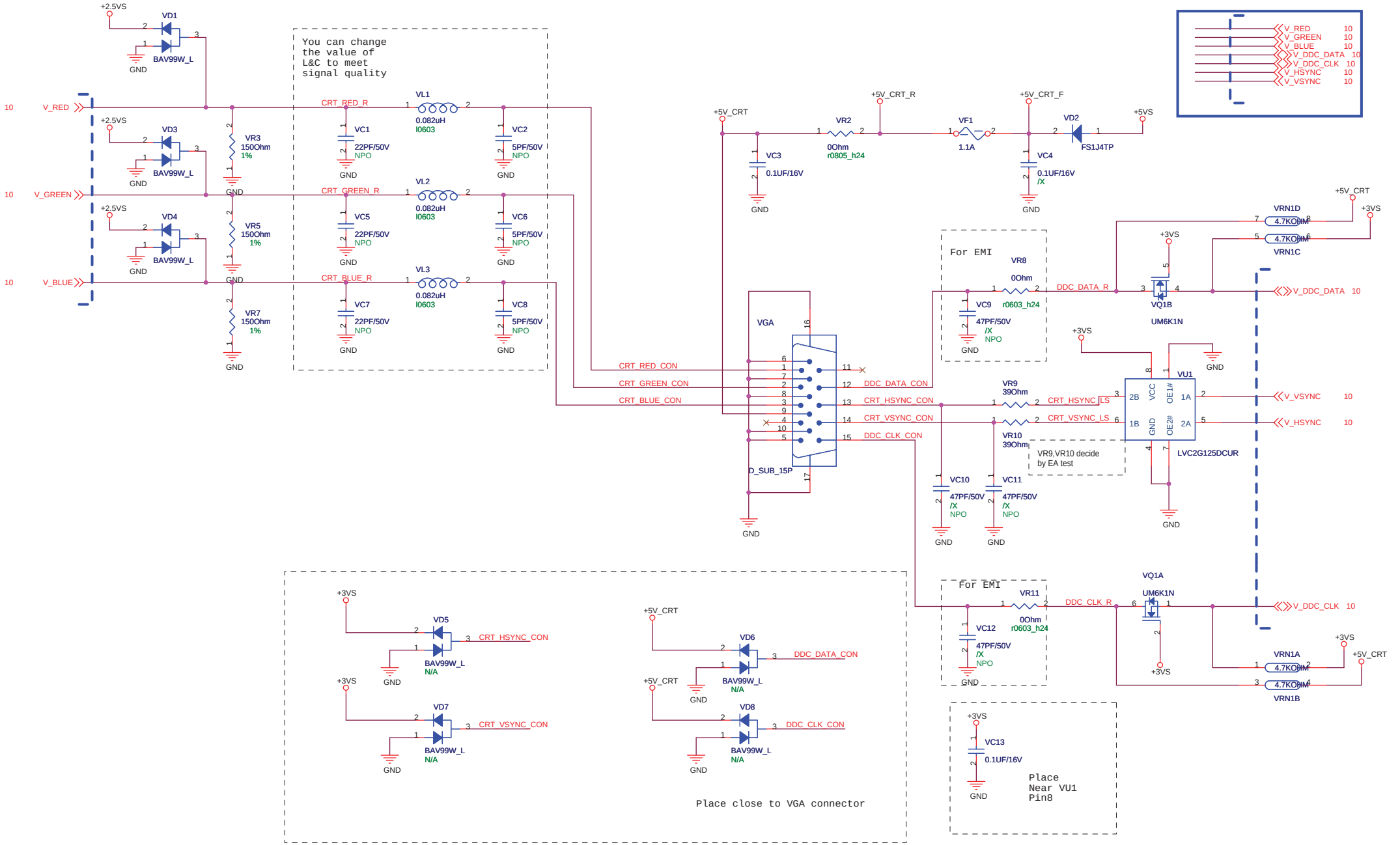




<Variant Name>

ASUSTek Computer INC.	Title : DDR2-Termination	
	Engineer: Endy_Wu	
Size: A3	Project Name: Standard Circuit	Rev: 0.1B
Date: Thursday, March 19, 2009	Sheet 21 of 48	

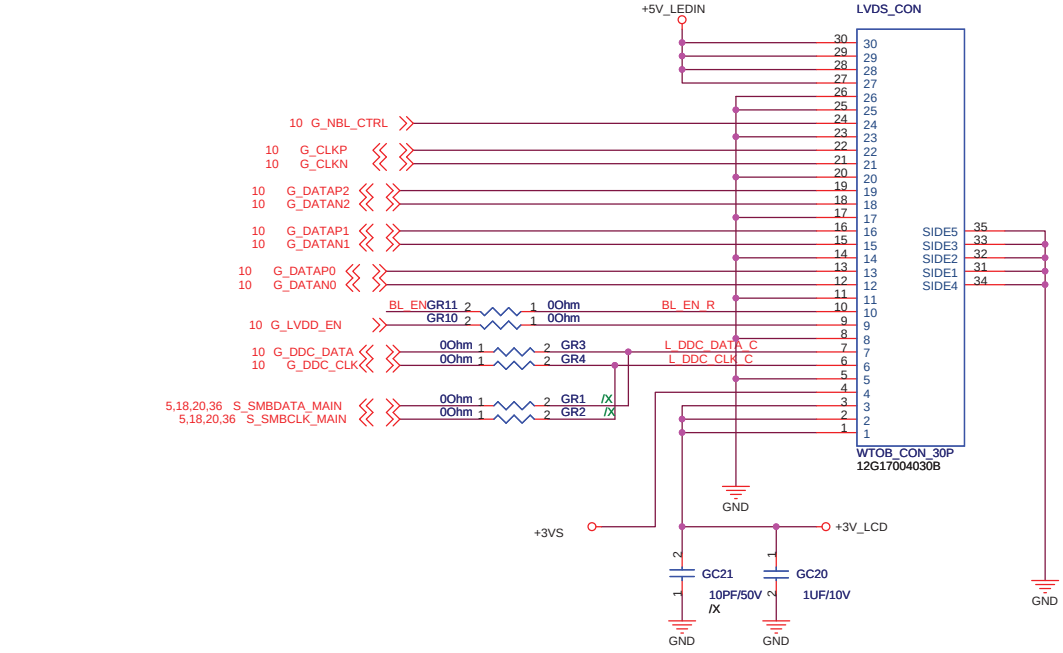
0.1D Beta

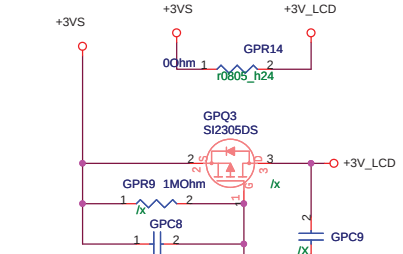


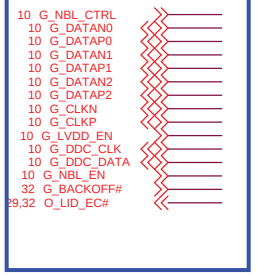
<Variant Name>

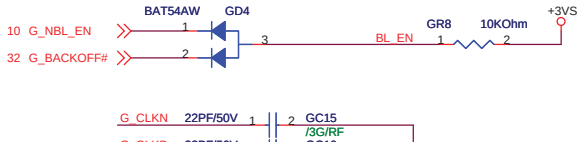
ASUSTek Computer INC.	Title : Onboard-VGA	
	Engineer: Susan_Shi	
Size: A3	Project Name: Standard Circuit	Rev: 0.1D
Date: Thursday, March 19, 2009	Sheet 22 of 48	

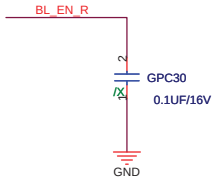
0.1 B Beta

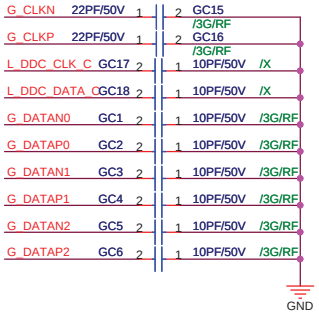


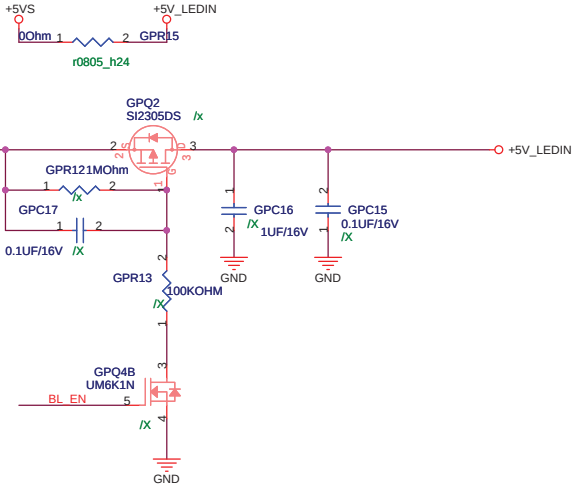


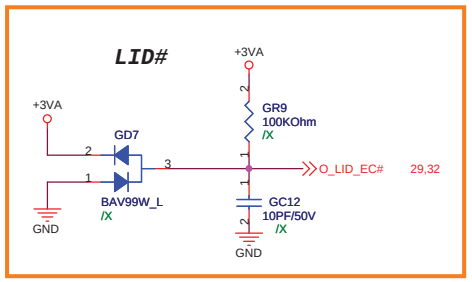


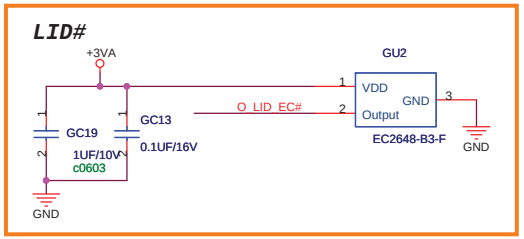








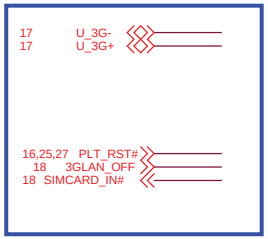




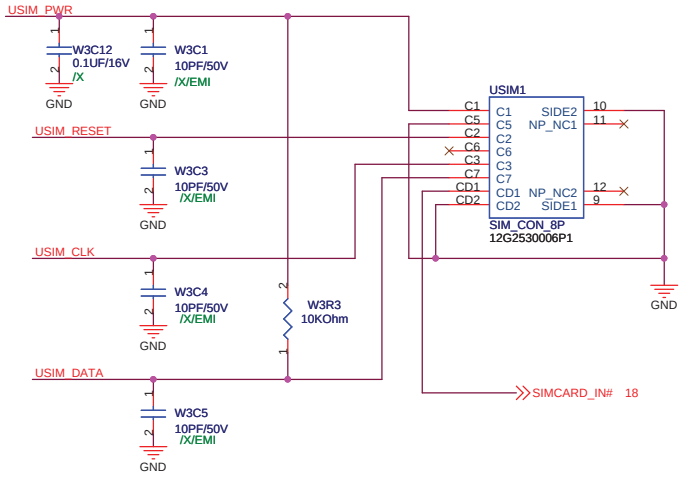
<Variant Name>

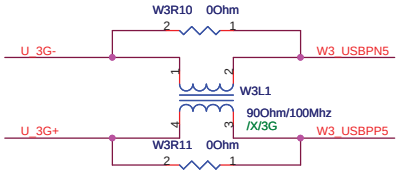
ASUSTek Computer Inc.	Title : LCD-CON DEMO	
	Engineer:	
Size: A3	Project Name	Rev: 0.1B
Date: Thursday, March 19, 2009	Sheet 23 of 48	

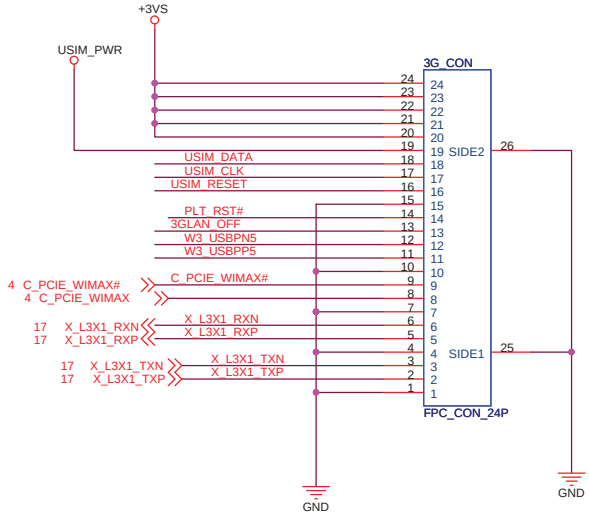
0.1A Beta



CAP Near SIM Socket







<Variant Name>

ASUSTek Computer INC.

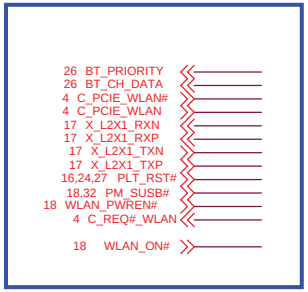
Title : 3G and WIMAX

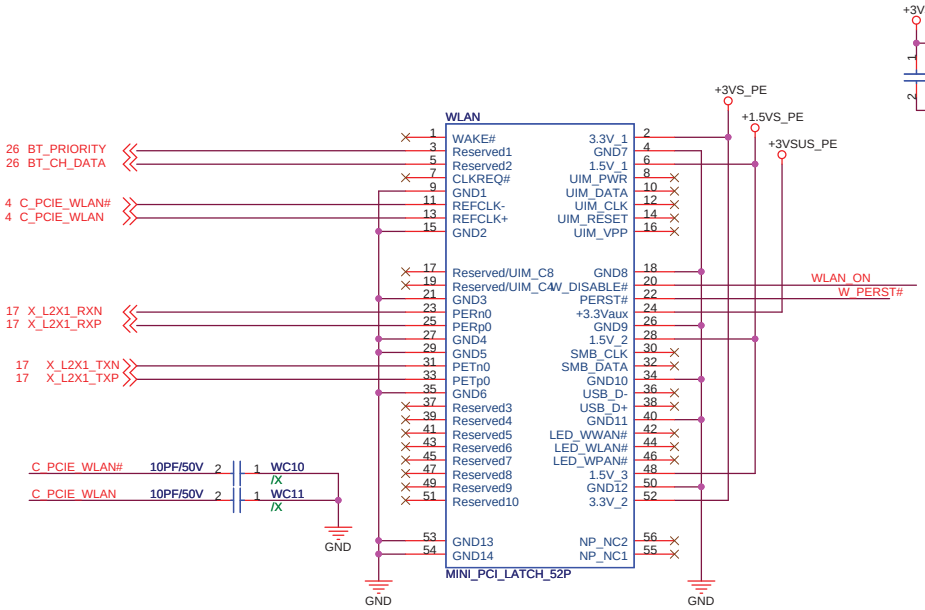
Engineer:

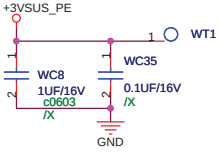
Size	Project Name	Rev
A3		0.1A

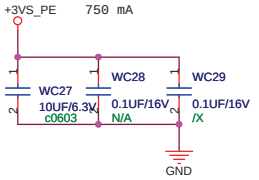
Date: Thursday, March 19, 2009 Sheet 24 of 48

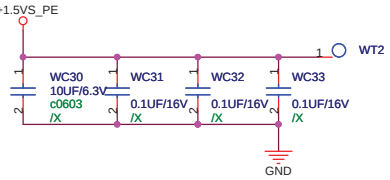
0.1C Beta

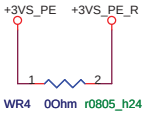


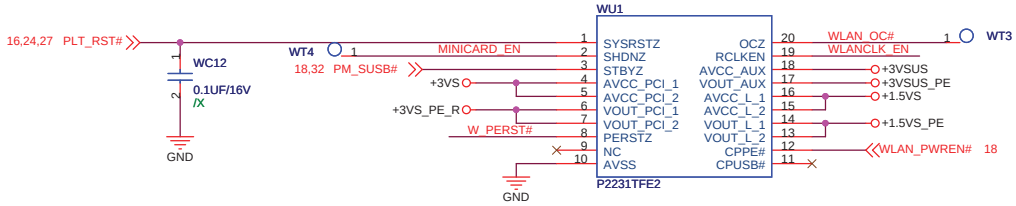


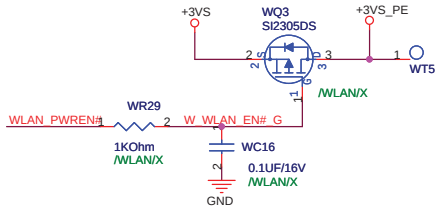


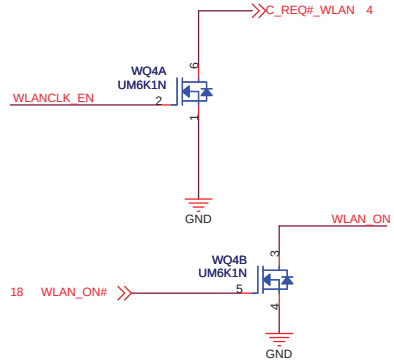


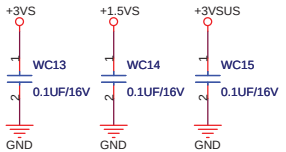






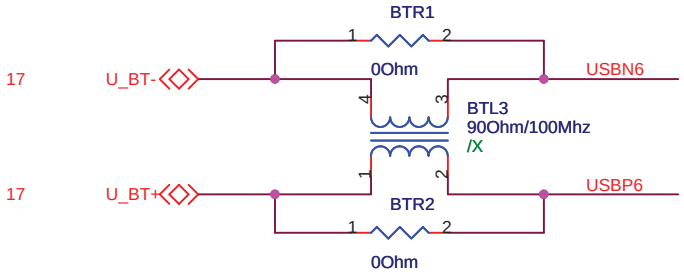


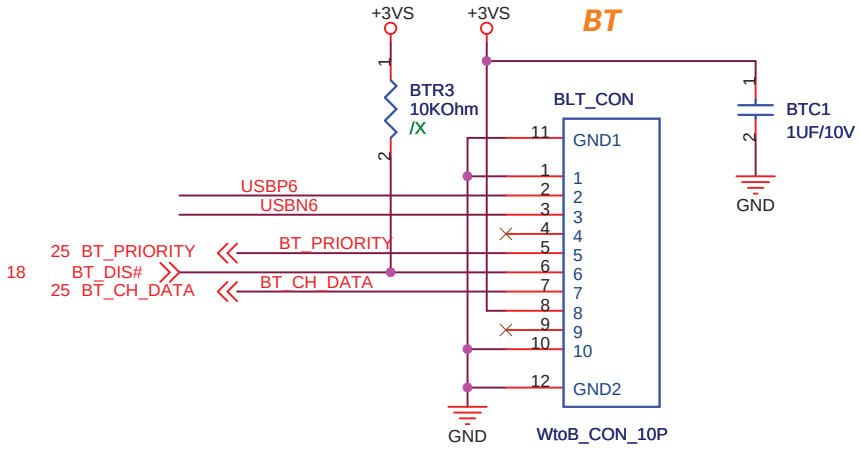




<Variant Name>

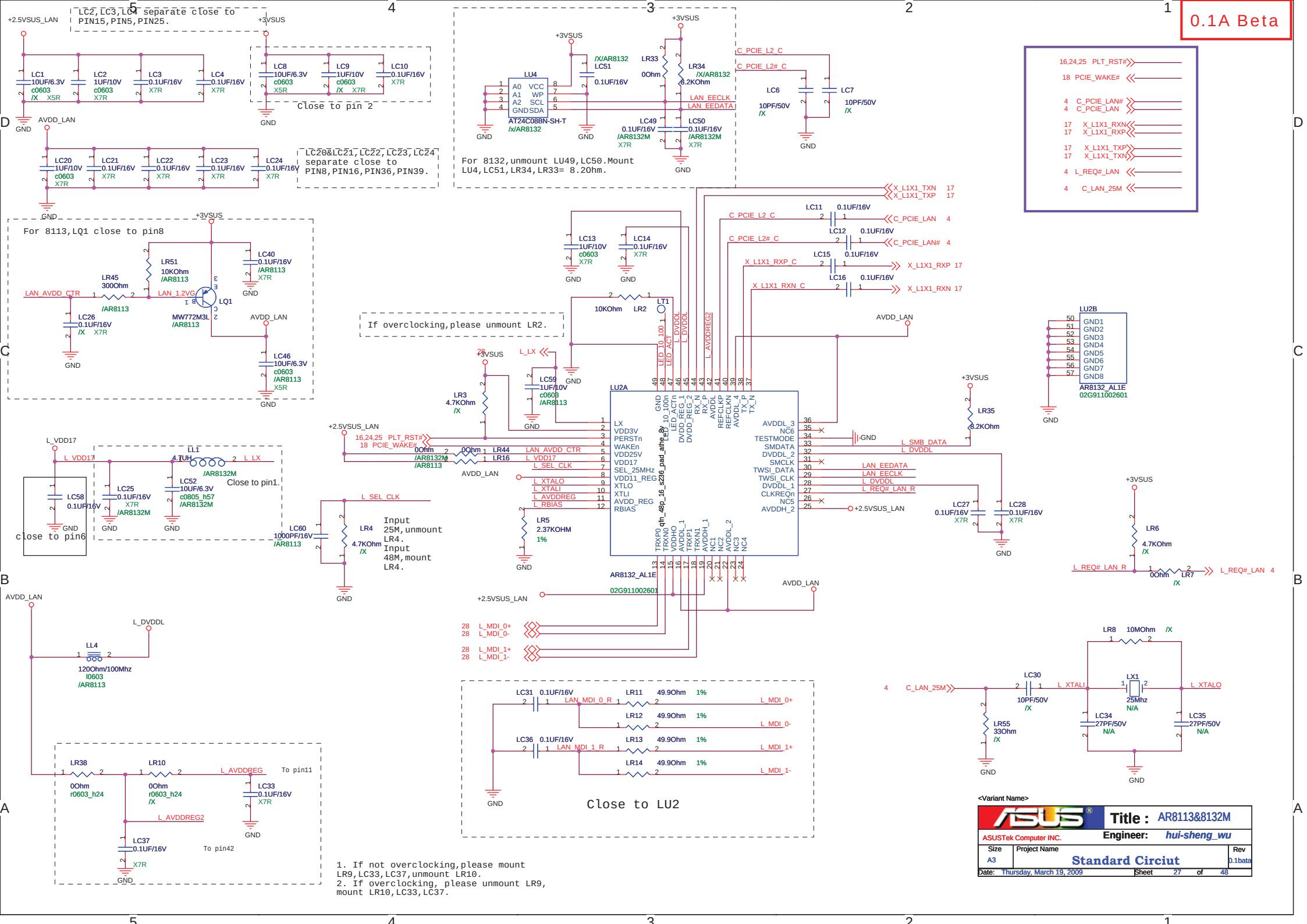
ASUSTek Computer INC.	Title : WLAN	
	Engineer: Joe1_Zhou	
Size: A3	Project Name: Standard circuit	Rev: 0.1C
Date: Thursday, March 19, 2009	Sheet 25 of 48	



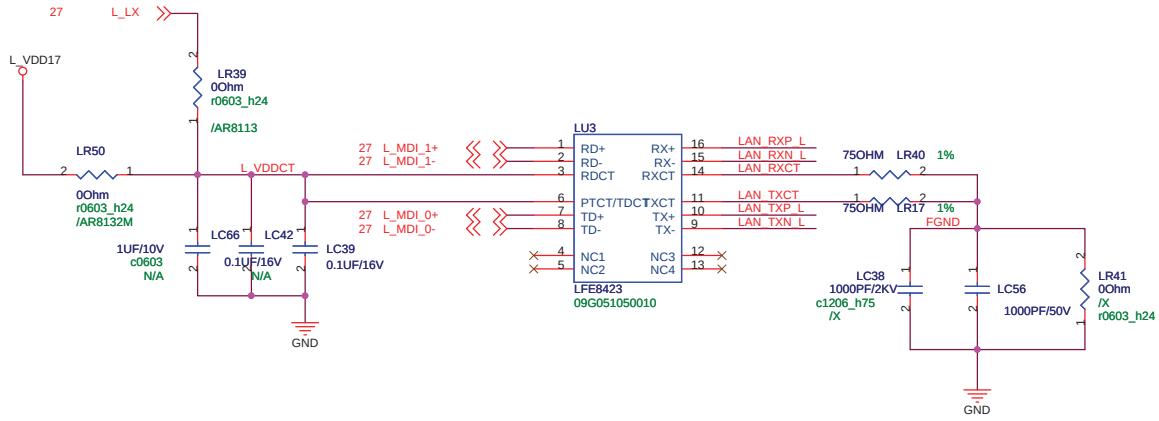


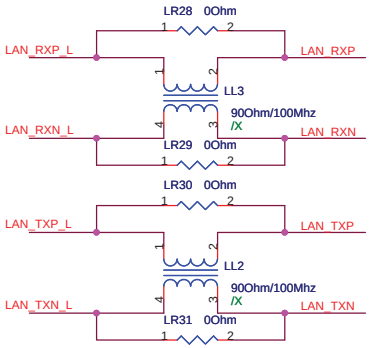
<Variant Name>

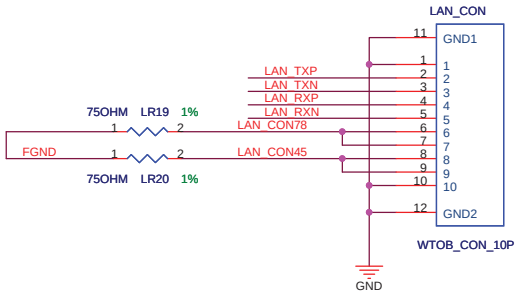
ASUSTek Computer INC.	Title : BLUETOOTH	
	Engineer: JOE1_ZHOU	
Size: A4	Project Name: Standard Circiut	Rev: 0.1A
Date: Thursday, March 19, 2009	Sheet 26 of 48	


0.1A Beta
LC2,LC3,LC4 separate close to PIN15,PIN5,PIN25.
Close to pin 2
LC20&LC21,LC22,LC23,LC24 separate close to PIN8,PIN16,PIN36,PIN39.
For 8132,unmount LU49,LC50.Mount LU4,LC51,LR34,LR33= 8.2Ohm.
For 8113,LQ1 close to pin8
If overclocking,please unmount LR2.
close to pin6
Close to pin1.
Input 25M,unmount LR4. Input 48M,mount LR4.
To pin11
To pin42
Close to LU2
1. If not overclocking,please mount LR9,LC33,LC37,unmount LR10.
2. If overclocking, please unmount LR9, mount LR10,LC33,LC37.
<Variant Name>
Title : AR8113&8132M
ASUSTek Computer INC.
Engineer: hui-sheng_wu
Size A3
Project Name Standard Circiut
Rev 0.1bata
Date: Thursday, March 19, 2009
Sheet 27 of 48

0.1A Beta

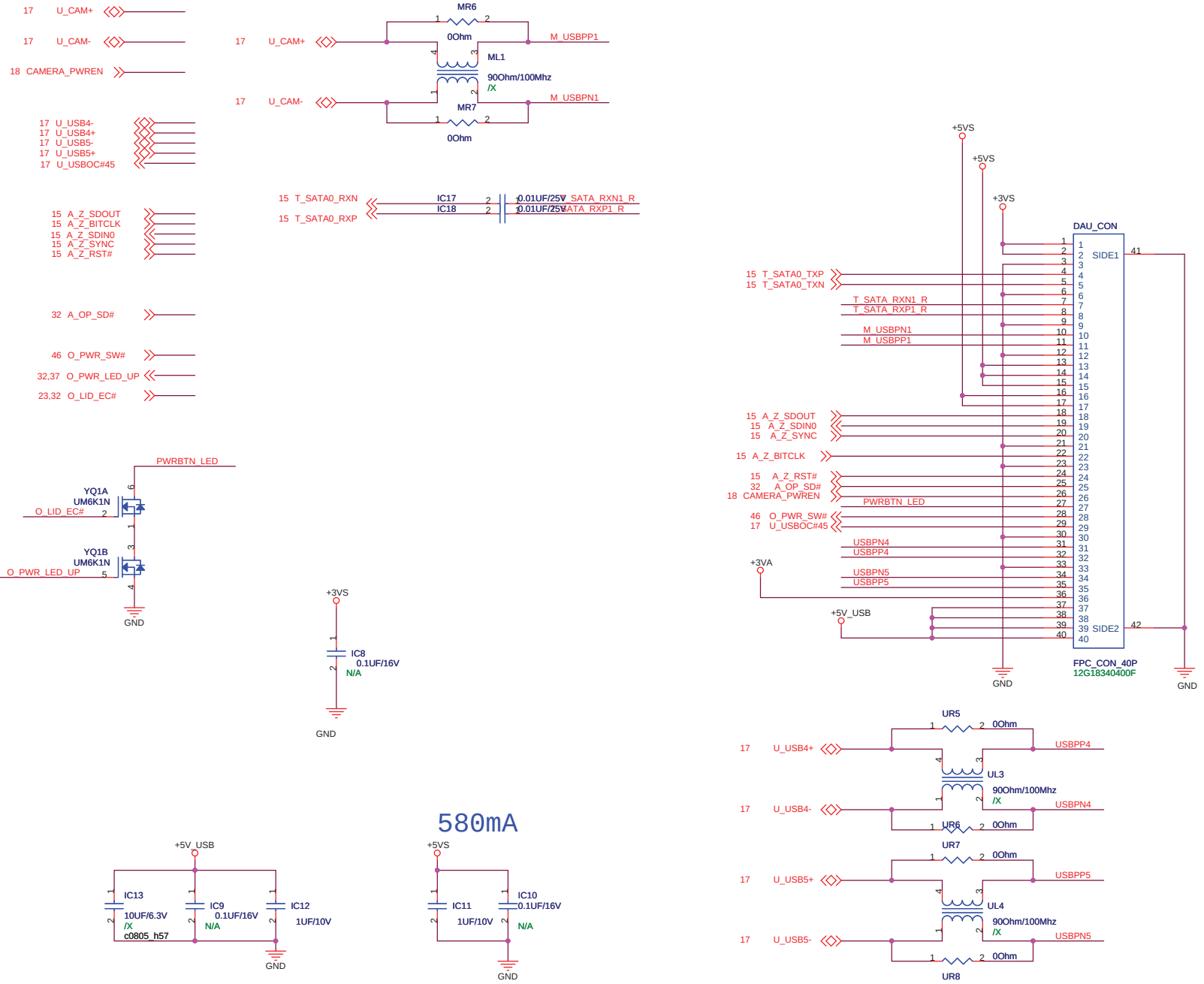






<Variant Name>

ASUSTek Computer INC.	Title : RJ45	
	Engineer: Hui-sheng_wu	
Size: A3	Project Name: Standard Circiut	Rev: 0.1A
Date: Thursday, March 19, 2009	Sheet 28 of 48	



<Variant Name>

ASUSTek Computer INC.

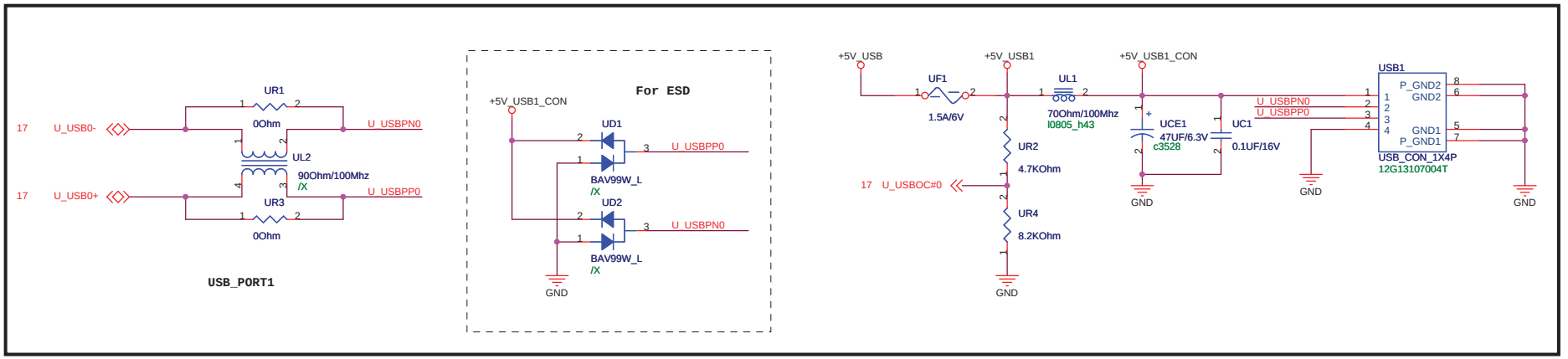
Title : SATA HDD

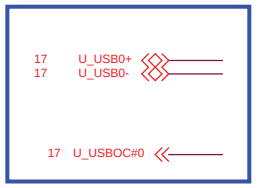
Engineer: KingCa_Jin

Size	Project Name	Rev
A3	1000HN	1.0

Date: Thursday, March 19, 2009 Sheet 29 of 48

0.1B Beta





<Variant Name>

ASUSTEK COMPUTER INC	Title : USB Port	
	Engineer: JOE1_ZHOU	
Size: A3	Project Name: Standard Circiut	Rev: 0.1B
Date: Thursday, March 19, 2009	Sheet 30 of 48	

<Variant Name>

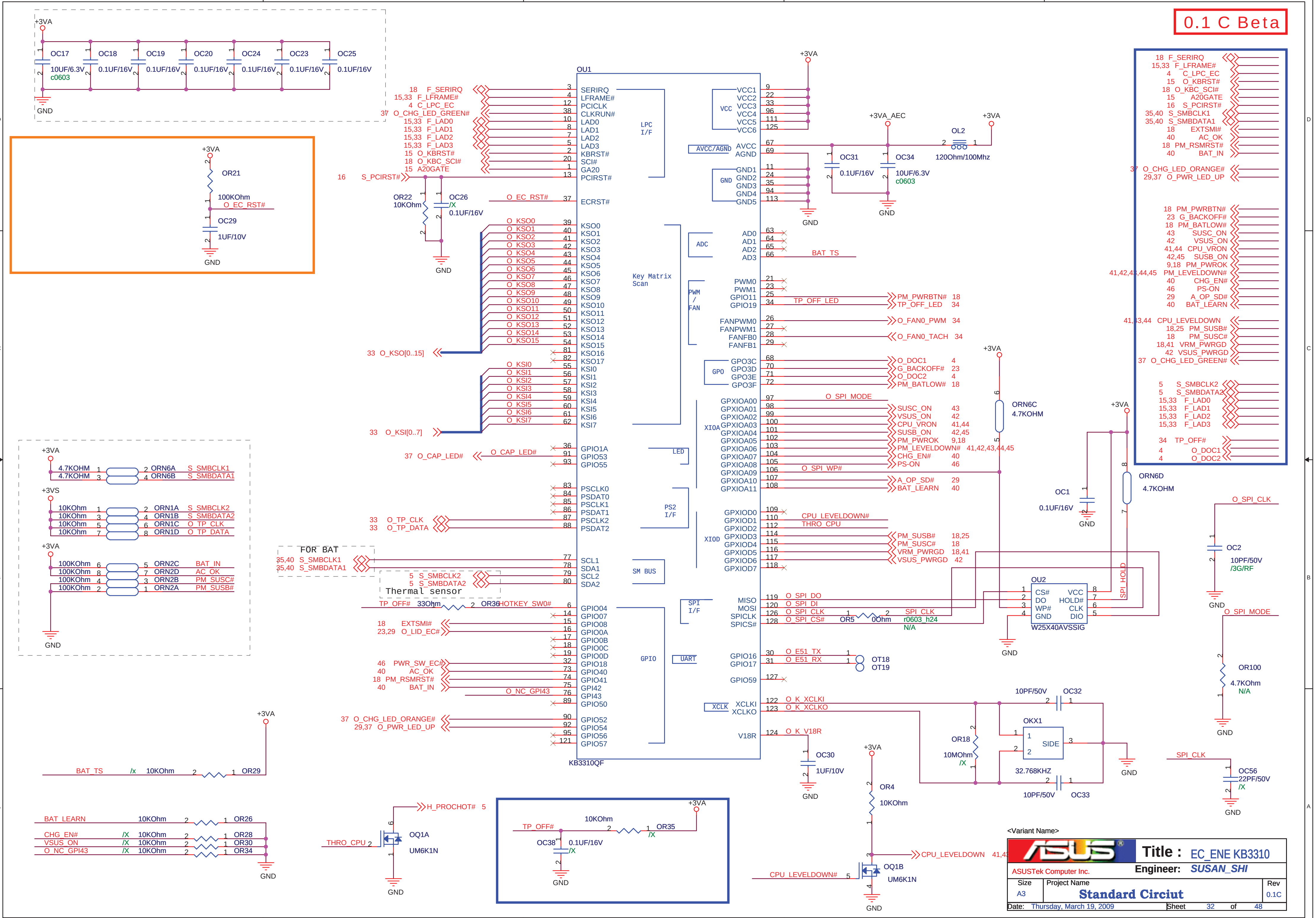
Title : Camera CONN

ASUSTEK COMPUTER INC

Engineer: KEN_JIN

Size	Project Name	Rev
A3	Standard Circiut	0.1A

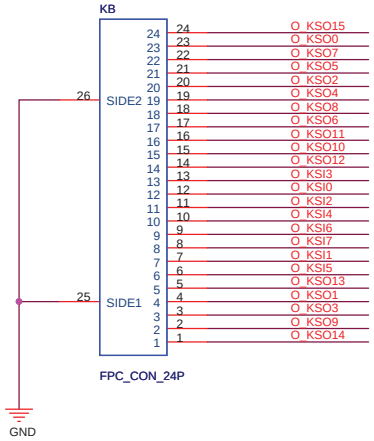
Date: Thursday, March 19, 2009 Sheet 31 of 48

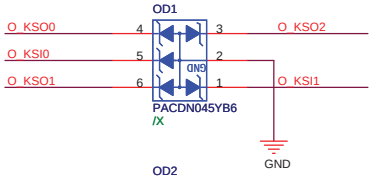


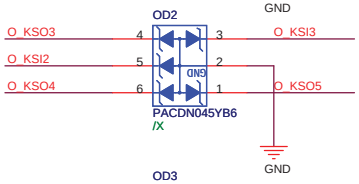
0.1 C Beta
OU1
KB3310QF
SERIRQ
LFRAME#
PCICLK
CLKRUN#
LAD0
LAD1
LAD2
LAD3
KBRST#
SCI#
GA20
PCIRST#
ECRST#
LPC I/F
Key Matrix Scan
ADC
PWM / FAN
GPO
XIOA
XIOD
LED
PS2 I/F
SM BUS
SPI I/F
UART
GPIO
XCLK
VCC
AVCC/AGND
GND
FOR BAT
Thermal sensor
OU2
W25X40AVSSIG
OKX1
32.768KHZ
OQ1A
UM6K1N
OQ1B
UM6K1N
OL2
120Ohm/100Mhz
+3VA
+3VS
+3VA_AEC
GND
<Variant Name>
Title : EC_ENE KB3310
ASUSTek Computer Inc.
Engineer: SUSAN_SHI
Size A3
Project Name
Standard Circuit
Rev 0.1C
Date: Thursday, March 19, 2009
Sheet 32 of 48

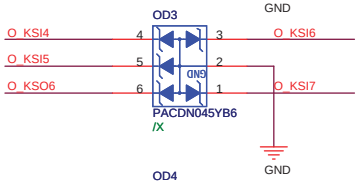
O_KSO[0..15] 32
O_KSI[0..7] 32

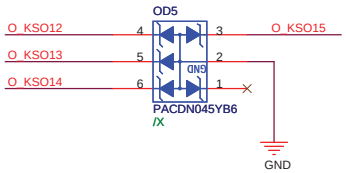
For Keyboard Connector

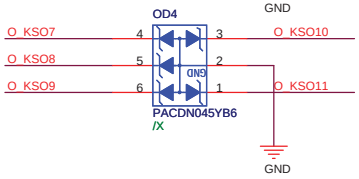


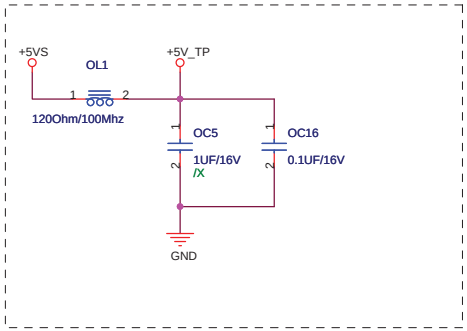


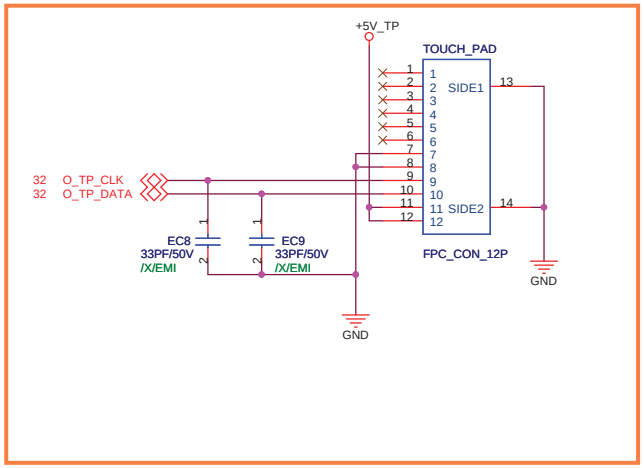


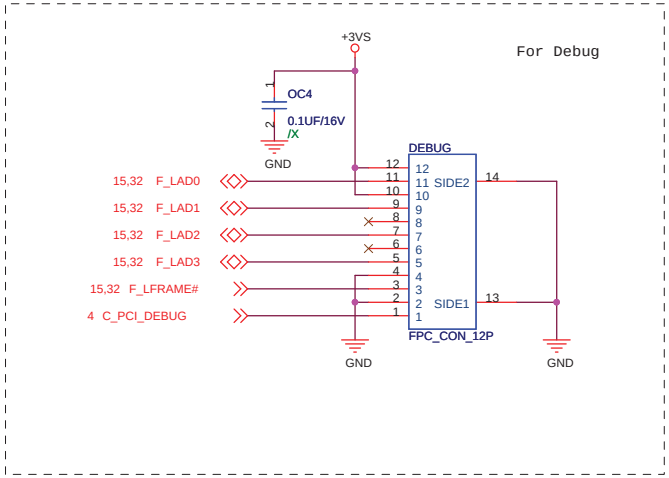


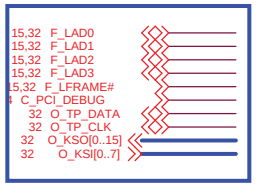






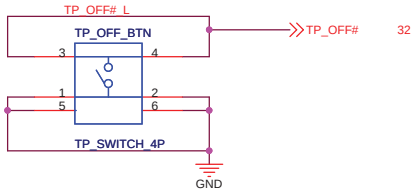


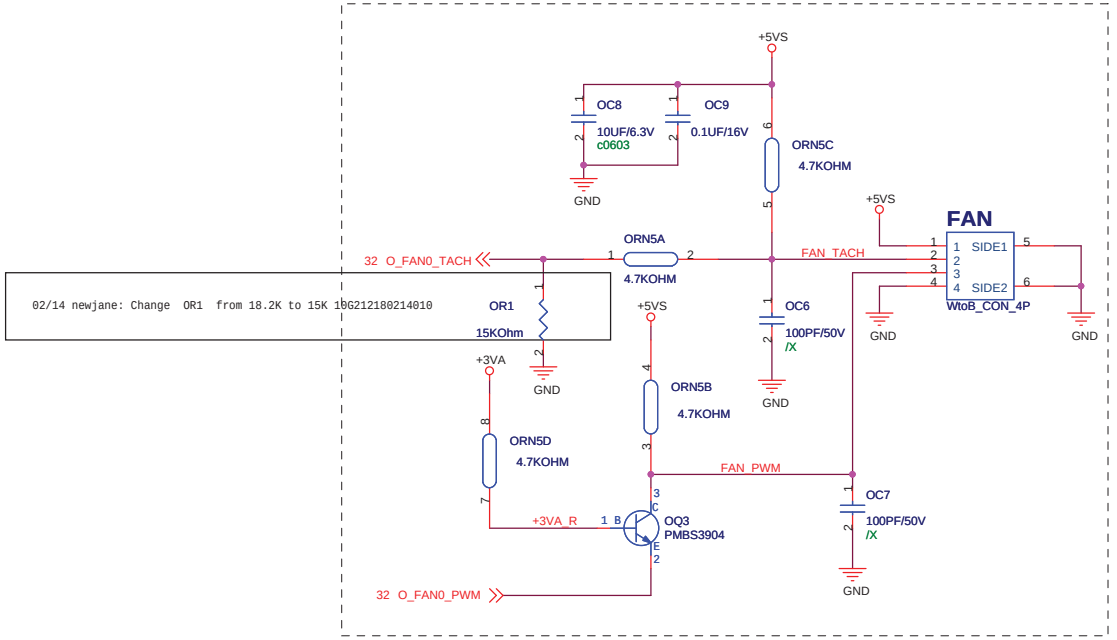




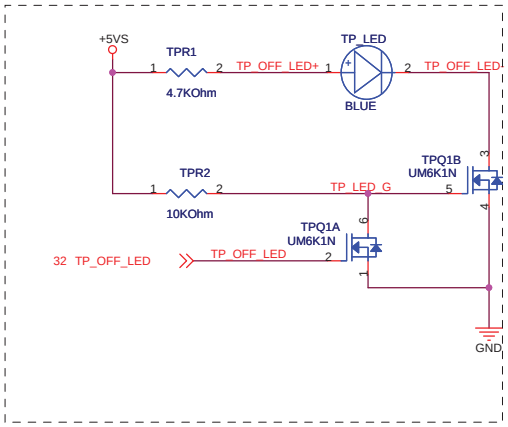
<Variant Name>

ASUSTek Computer Inc.	Title : EC_ENE KB3310	
	Engineer: SUSAN_SHI	
Size: A3	Project Name: Standard Circiut	Rev: 0.1C
Date: Thursday, March 19, 2009	Sheet 33 of 48	





For TP LED

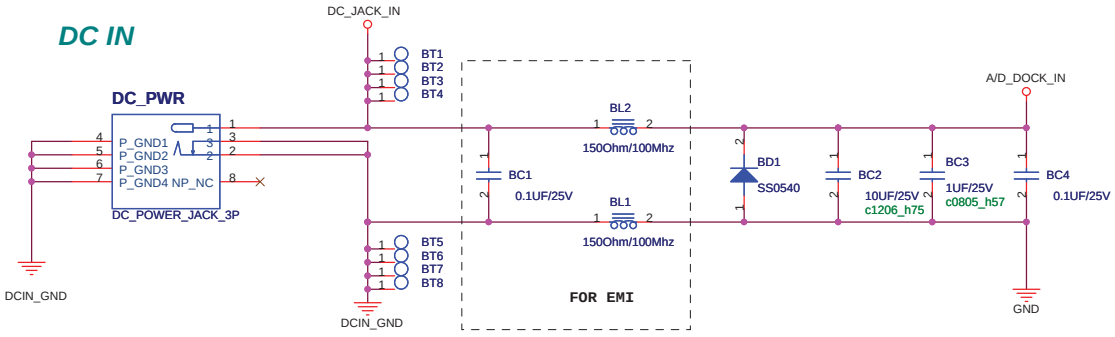


<Variant Name>

ASUSTek Computer Inc.	Title : EC_ENE KB3310	
	Engineer: SUSAN_SHI	
Size: A3	Project Name: Standard Circiut	Rev: 0.1C
Date: Thursday, March 19, 2009	Sheet 34 of 48	

0.1B Beta

DC IN

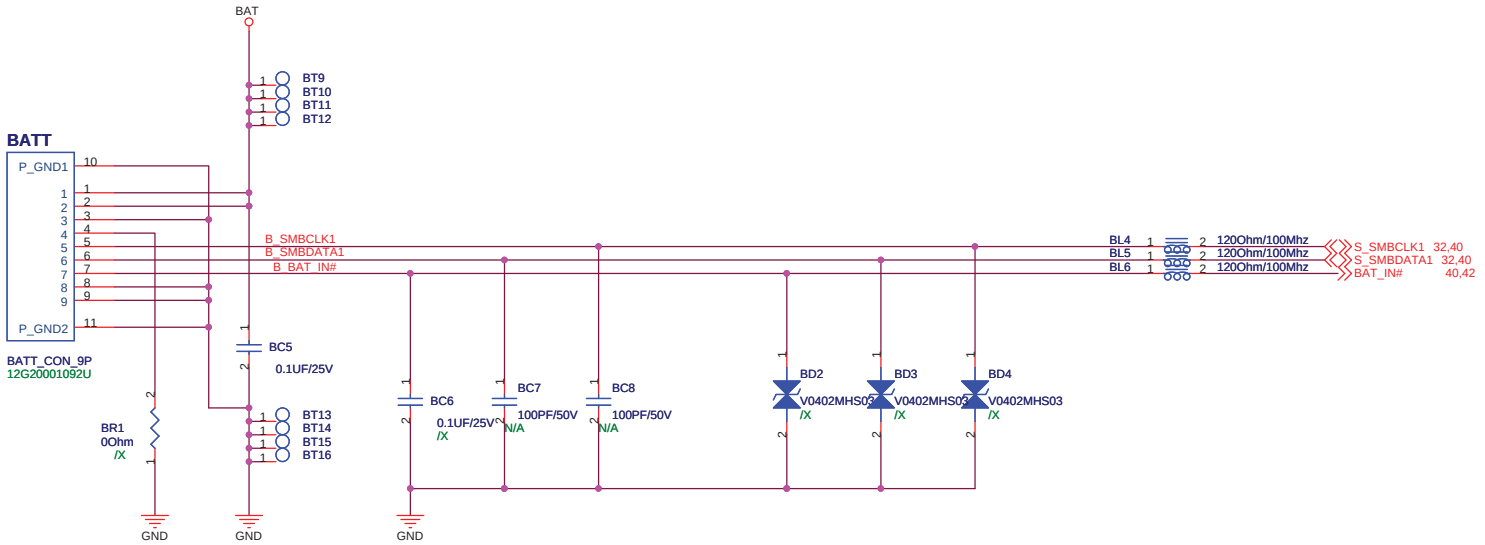


BAT_IN# 40,42

S_SMBCLK1 32,40

S_SMBDATA1 32,40

change from DIP to SMD

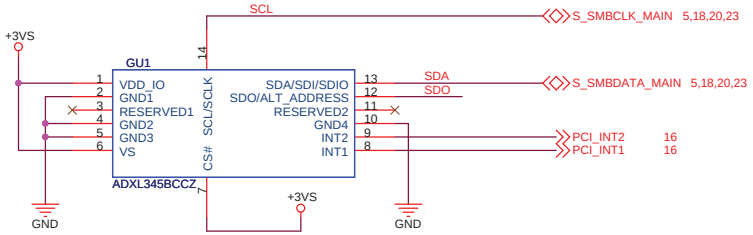


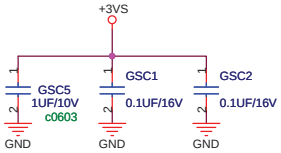
<Variant Name>

ASUSTEK COMPUTER INC	Title : PWR Jack	
	Engineer: KEN_JIN	
Size: A3	Project Name: Standard Circiut	Rev: 0.1B
Date: Thursday, March 19, 2009	Sheet 35 of 48	

0.1 A Beta

5,18,20,23 S_SMBCLK_MAIN
5,18,20,23 S_SMBDATA_MAIN
16 PCI_INT2
16 PCI_INT1





Install GSR6 being slave addrress "3A" for ADI/Freescale/ST G-sensors

<Variant Name>

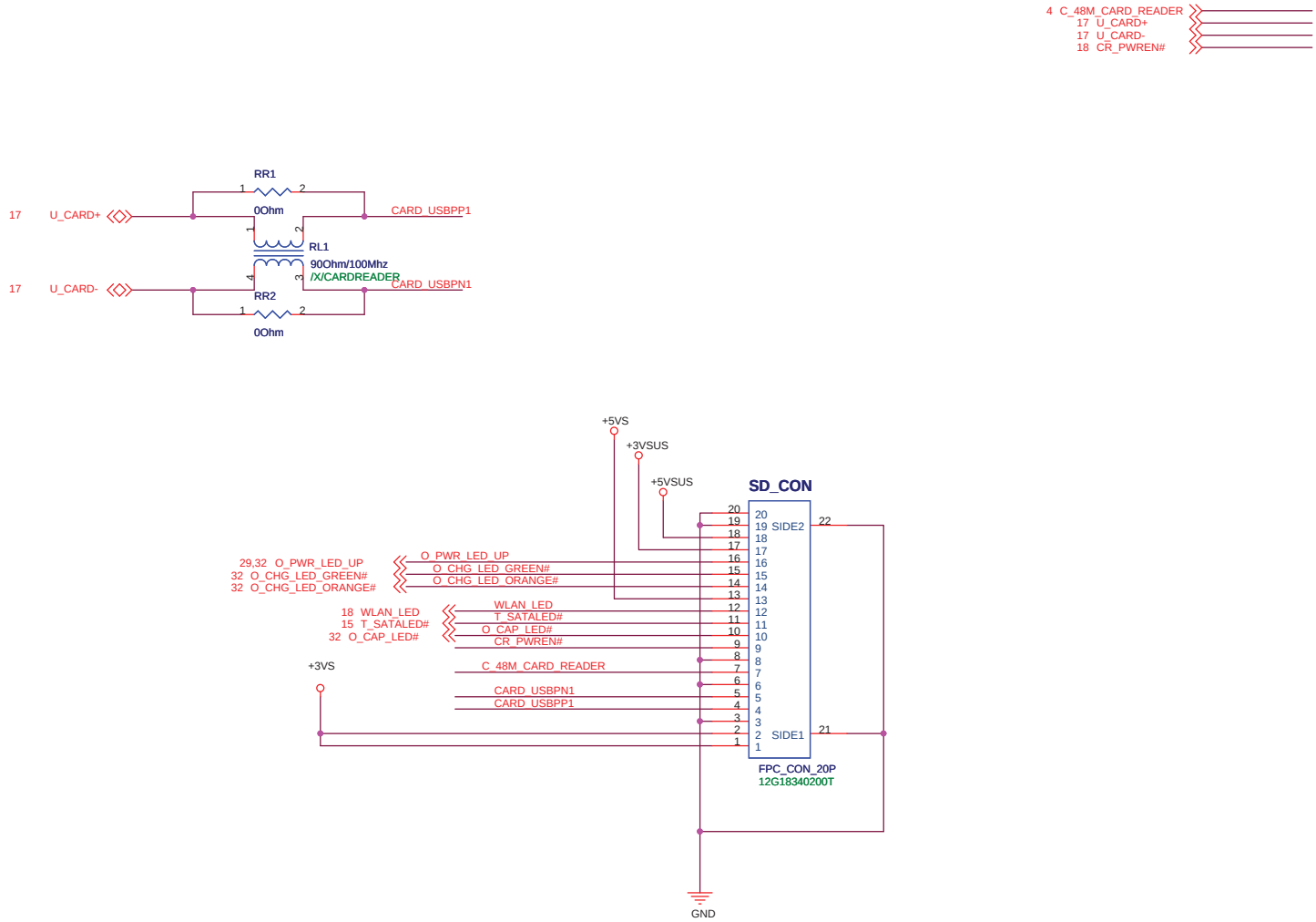
ASUSTek Computer Inc.

Title : G_sensor

Engineer: SUSAN_SHI

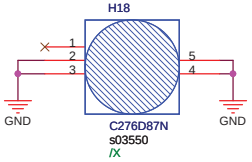
Size	Project Name	Rev
A3	Standard Circiut	0.1A

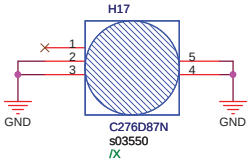
Date: Thursday, March 19, 2009 Sheet 36 of 48

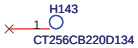


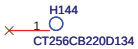
<Variant Name>

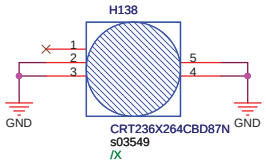
<OrgName>	Title : <Title>	
	Engineer: Lus Lu	
Size: A3	Project Name: <Doc>	Rev: 1.0
Date: Thursday, March 19, 2009	Sheet 37 of 48	

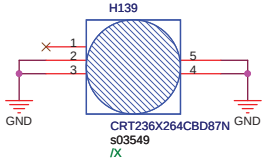


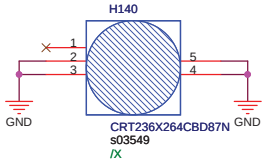


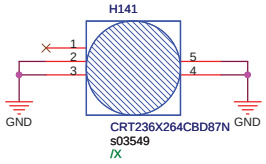


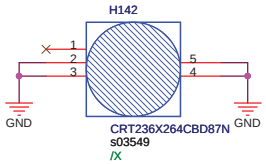












<Variant Name>

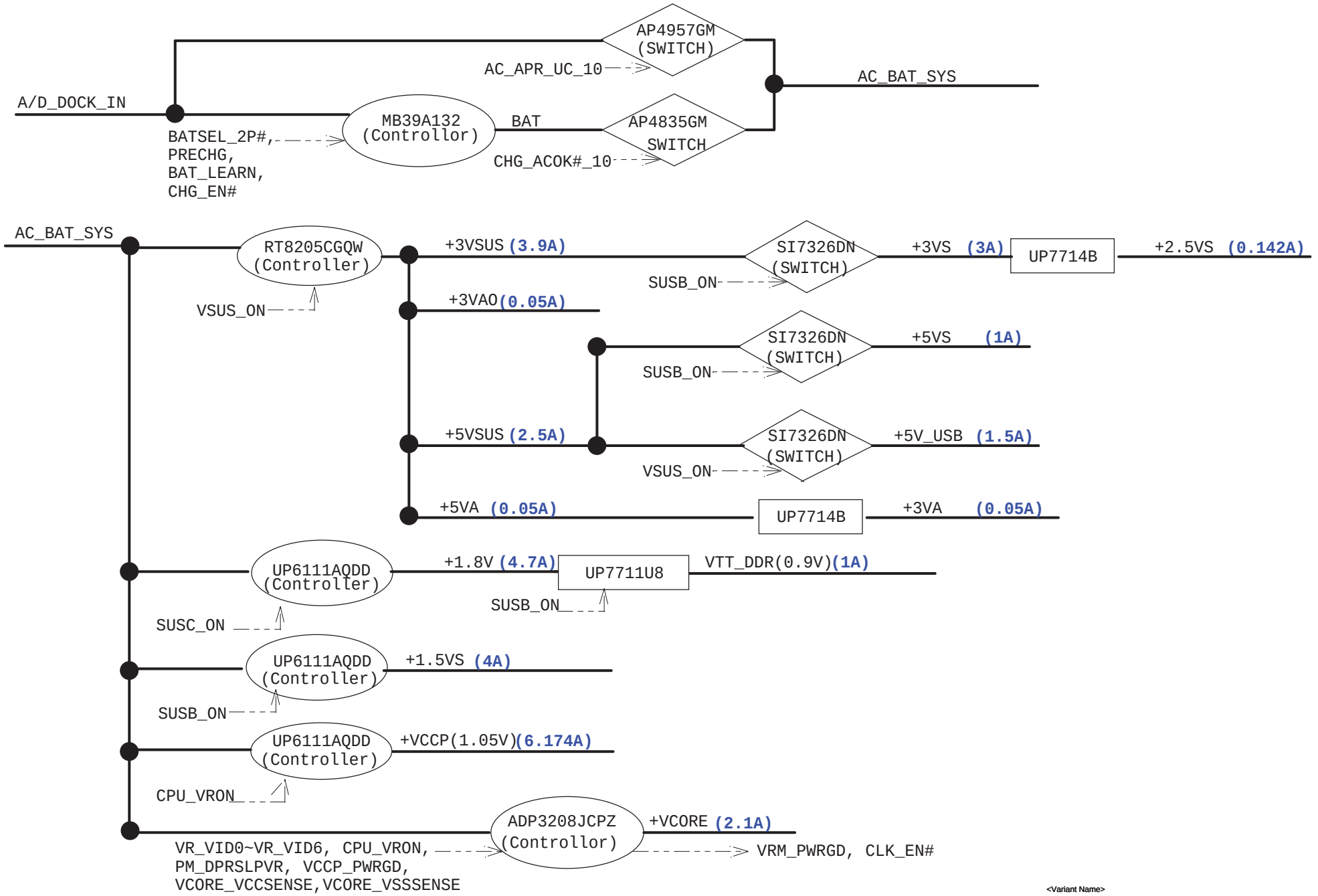
ASUSTek Computer INC.

Title : Srew Hole

Engineer: Kell_Huang

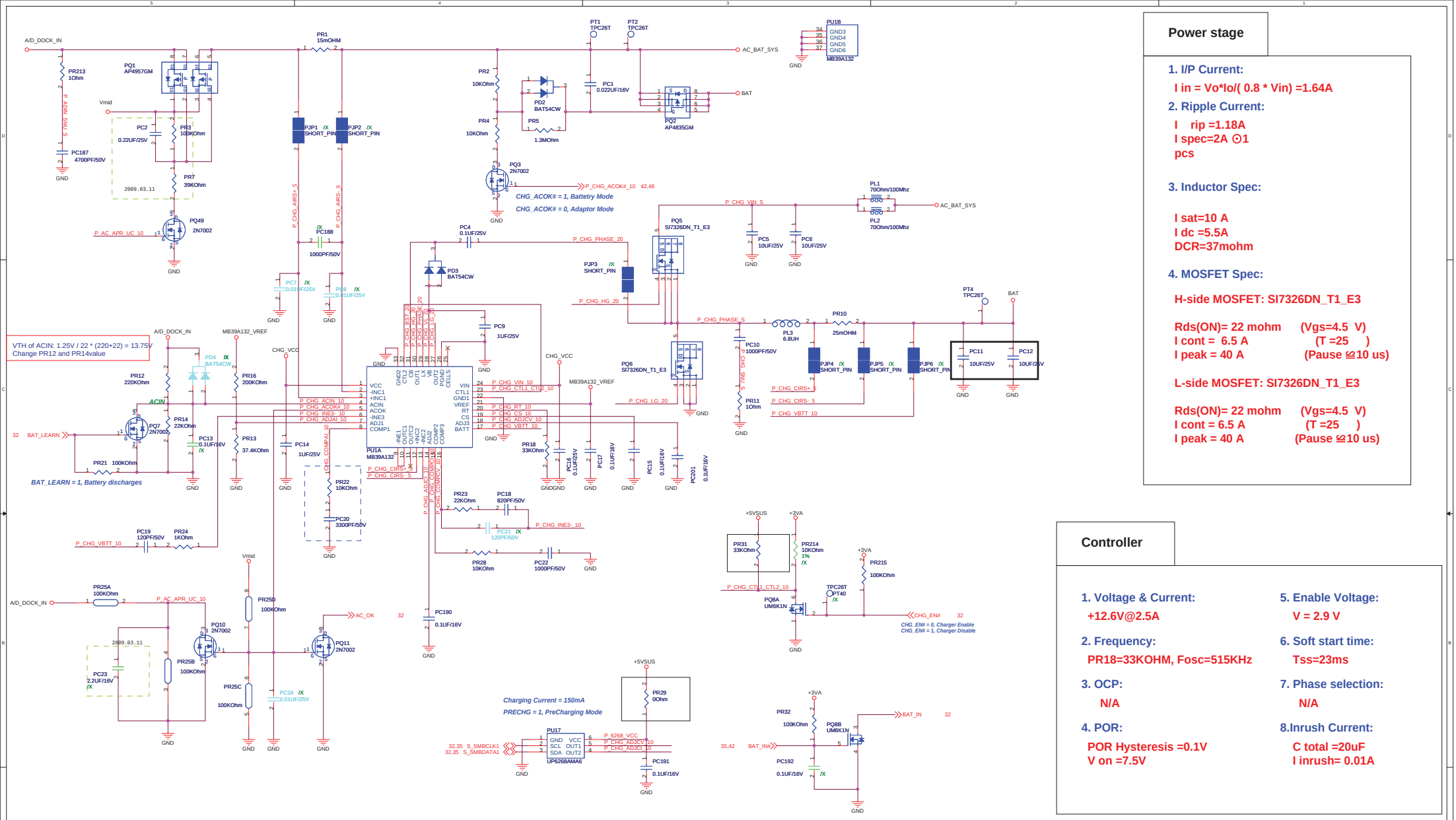
Size	Project Name	Rev
A3	1005HN_MN	1.0G

Date: Thursday, March 19, 2009 Sheet 38 of 48



<Variant Name>

ASUSTek Computer INC.	Title : Power Flow	
	Engineer: Joy_Zhou	
Size: A3	Project Name: 1005HA	Rev: 1.0
Date: Thursday, March 19, 2009	Sheet 39 of 48	



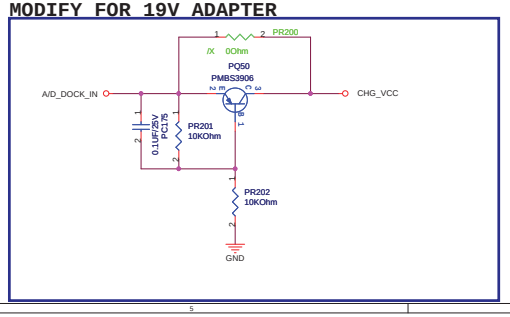
Power stage

1. I/P Current:
   I in = Vo*Io/(0.8 * Vin) =1.64A
2. Ripple Current:
   I rip =1.18A
   I spec=2A ⊙1
   pcs
3. Inductor Spec:
   I sat=10 A
   I dc =5.5A
   DCR=37mohm
4. MOSFET Spec:
   H-side MOSFET: SI7326DN_T1_E3
   Rds(ON)= 22 mohm (Vgs=4.5 V)
   I cont = 6.5 A (T =25)
   I peak = 40 A (Pause ≦10 us)
   L-side MOSFET: SI7326DN_T1_E3
   Rds(ON)= 22 mohm (Vgs=4.5 V)
   I cont = 6.5 A (T =25)
   I peak = 40 A (Pause ≦10 us)

Controller

1. Voltage & Current:
   +12.6V@2.5A
2. Frequency:
   PR18=33KOHM, Fosc=515KHz
3. OCP:
   N/A
4. POR:
   POR Hysteresis =0.1V
   V on =7.5V
5. Enable Voltage:
   V = 2.9 V
6. Soft start time:
   Tss=23ms
7. Phase selection:
   N/A
8. Inrush Current:
   C total =20uF
   I inrush= 0.01A

MODIFY FOR 19V ADAPTER



Battery Charging Current :

4.4V > Vadj2 >= 0V ==>
Ichg = (Vadj2-0.075)/(25*Rs)
BATSEL_2P# = 1, Ich=1.49A
BATSEL_2P# = 0, Ich=2.5A

Input Adaptor Max. Current Limit :

Ilimit_current = (Vadj1-0.075) / (25*Rs)=1.90A

Pre-Charging Mode :

Precharging current = 149.2mA

Vadj2 = 168mV

ACIN Threshold = 1.25V

Adaptor > 13.75V, System Powered by Adaptor

Adaptor <13.75V, System Powered by Battery

Battery Charging Voltage :

Vadj3 :VREF ==> Vbat = 4.2V /cell
3.9V>Vadj3>2.4V ==> Vbat = 4.35V/cell
Vadj3 :GND ==> Vbat = 4.0V /cell
2.2V>Vadj3>1.1V ==> Vbat = 2*Vadj3 /cell

Battery Cell Selection :

CELLS: VREF ==> 4 Cells;
CELLS: OPEN ==> 3 Cells;
CELLS: GND ==> 2 Cells;

VREF = 5.0V

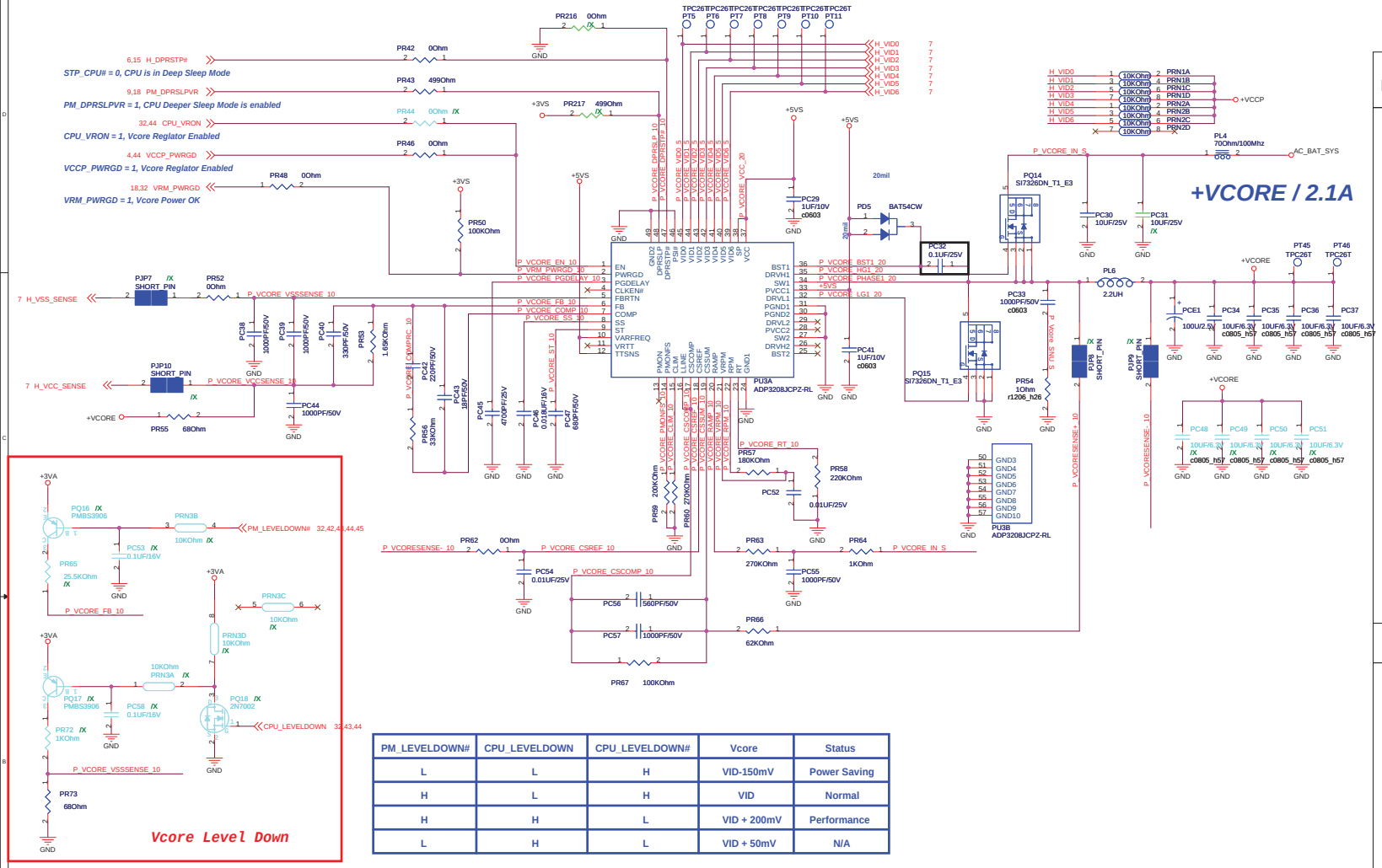
fosc(KHz) = 17000 / RT (KOhm)
=515KHz

*Soft start: ts(s) = 0.13 * CS (uF)*

<Variant Name>

ASUSTek Computer INC.

Title : Charger
Engineer: Joy_Zhou
Size: A2 | Project Name: 1005HA | Rev: 1.0G
Date: Thursday, March 19, 2009 | Sheet 40 of 48



PM_LEVELDOWN#	CPU_LEVELDOWN	CPU_LEVELDOWN#	Vcore	Status
L	L	H	VID-150mV	Power Saving
H	L	H	VID	Normal
H	H	L	VID + 200mV	Performance
L	H	L	VID + 50mV	N/A

Power Stage

1. I/P Current:
   - I in = Vo*Io/(0.8 * Vin) =0.32A
2. Ripple Current:
   - I rip =0.6A
   - I spec=2.5A
3. Dynamic:
   - ~~Q1pcs~~
   - I peak=2.1 A
   - ESR / 1 pcs =18mohm
   - 〉V =38mV
4. Inductor Spec:
   - I sat=14 A
   - I dc =8 A
   - DCR=18 mohm
5. MOSFET Spec:

H-side MOSFET: SI7326DN_T1_E3

Rds(ON)= 22 mohm (Vgs=4.5 V)
I cont = 6.5 A (T =25)
I peak = 40 A (Pause ≦10 us)

L-side MOSFET: SI7326DN_T1_E3

Rds(ON)= 22 mohm (Vgs=4.5 V)
I cont = 6.5 A (T =25)
I peak = 40 A (Pause ≦10 us)

Controller

1. Voltage & Current:
   - VCORE=0.5-1.5V@2.1A
2. Frequency:
   - Set PR58=220Kohm
   - Fosc=322KHz for RPM
   - Set PR57=180Kohm
   - Fosc=272KHz for CCM
3. OCP:
   - Set PR60=270KOHM
   - Iocp=9.3A
4. POR:
   - POR Hysteresis =0.15V
   - V on =4.4-4.5 V
   - V off =4.0-4.2 V
5. UVP:
   - VID-300mV
6. OVP:
   - VID+200mV
7. Soft start time:
   - 2.7ms
8. Phase selection:
   - SP=VCC
   - sigle phase
9. Loadline:
   - 30mOhm

<Variant Name>

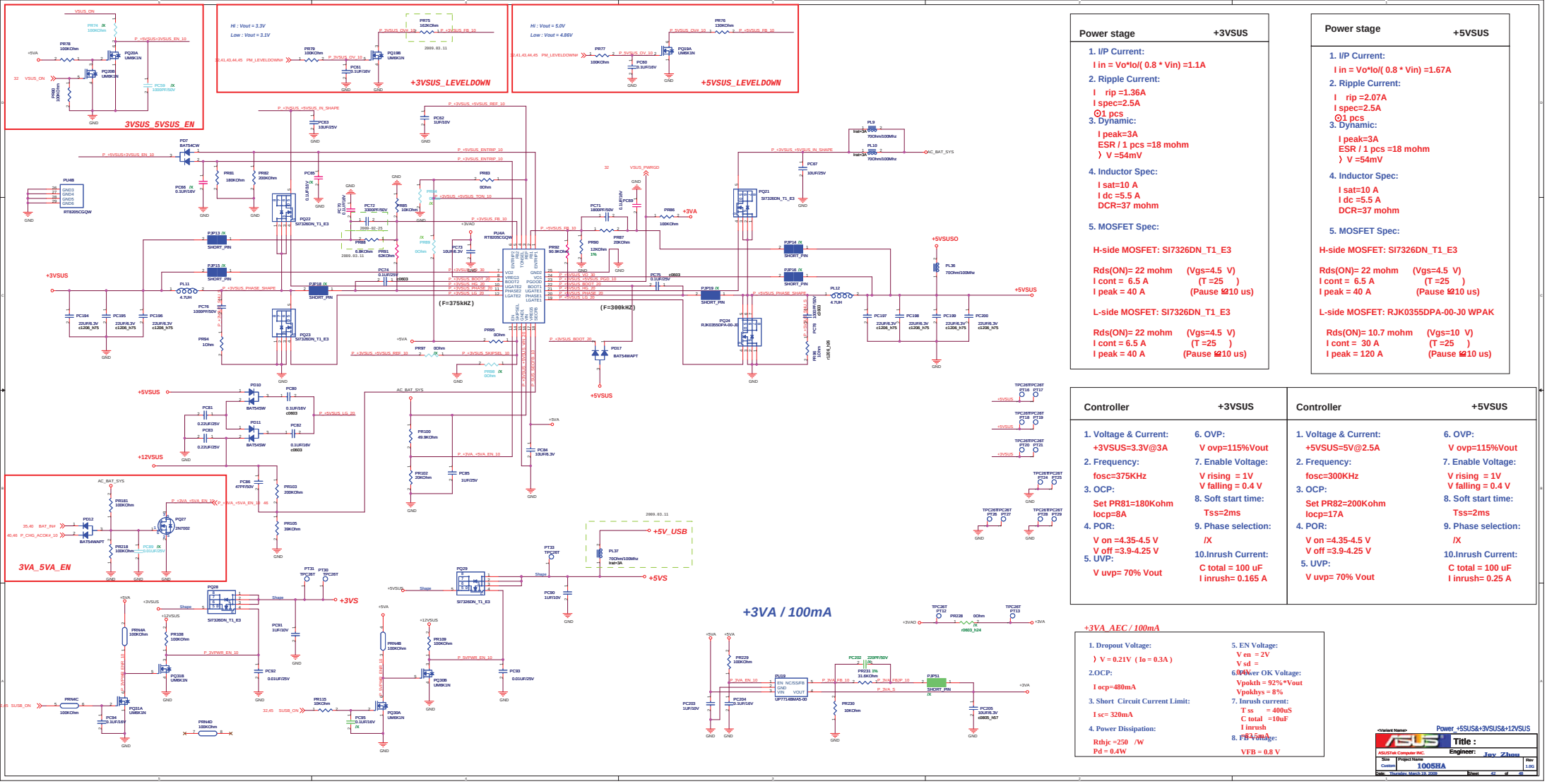
ASUSTek Computer INC.

Title : Vcore

Engineer: Joy_Zhou

Size	Project Name	Rev
A2	1005HA	1.3G

Date: Thursday, March 19, 2009 Sheet 41 of 48



Power stage +3VSUS

1. I/P Current:
   I in = Vo*Io/(0.8 * Vin) =1.1A
2. Ripple Current:
   I rip =1.36A
   I spec=2.5A
   ⊙1 pcs
3. Dynamic:
   I peak=3A
   ESR / 1 pcs =18 mohm
   ⟩ V =54mV
4. Inductor Spec:
   I sat=10 A
   I dc =5.5 A
   DCR=37 mohm
5. MOSFET Spec:

H-side MOSFET: SI7326DN_T1_E3

Rds(ON)= 22 mohm (Vgs=4.5 V)
I cont = 6.5 A (T =25)
I peak = 40 A (Pause ≦10 us)

L-side MOSFET: SI7326DN_T1_E3

Rds(ON)= 22 mohm (Vgs=4.5 V)
I cont = 6.5 A (T =25)
I peak = 40 A (Pause ≦10 us)

Power stage +5VSUS

1. I/P Current:
   I in = Vo*Io/(0.8 * Vin) =1.67A
2. Ripple Current:
   I rip =2.07A
   I spec=2.5A
   ⊙1 pcs
3. Dynamic:
   I peak=3A
   ESR / 1 pcs =18 mohm
   ⟩ V =54mV
4. Inductor Spec:
   I sat=10 A
   I dc =5.5 A
   DCR=37 mohm
5. MOSFET Spec:

H-side MOSFET: SI7326DN_T1_E3

Rds(ON)= 22 mohm (Vgs=4.5 V)
I cont = 6.5 A (T =25)
I peak = 40 A (Pause ≦10 us)

L-side MOSFET: RJK0355DPA-00-J0 WPAK

Rds(ON)= 10.7 mohm (Vgs=10 V)
I cont = 30 A (T =25)
I peak = 120 A (Pause ≦10 us)

Controller +3VSUS

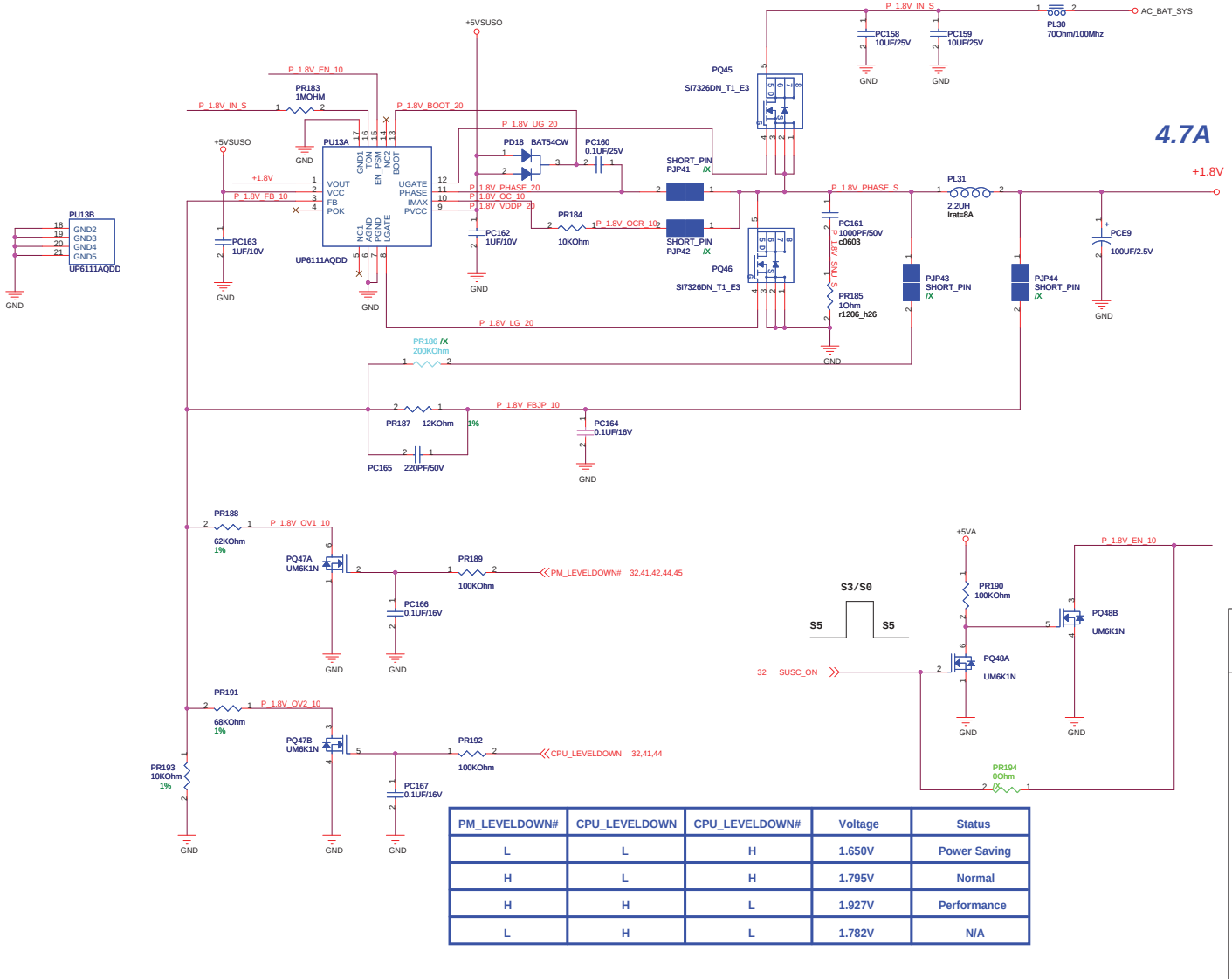
1. Voltage & Current:
   +3VSUS=3.3V@3A
2. Frequency:
   fosc=375KHz
3. OCP:
   Set PR81=180Kohm
   Iocp=8A
4. POR:
   V on =4.35-4.5 V
   V off =3.9-4.25 V
5. UVP:
   V uvp= 70% Vout
6. OVP:
   V ovp=115%Vout
7. Enable Voltage:
   V rising = 1V
   V falling = 0.4 V
8. Soft start time:
   Tss=2ms
9. Phase selection:
   /X
10. Inrush Current:
    C total = 100 uF
    I inrush= 0.165 A

Controller +5VSUS

1. Voltage & Current:
   +5VSUS=5V@2.5A
2. Frequency:
   fosc=300KHz
3. OCP:
   Set PR82=200Kohm
   Iocp=17A
4. POR:
   V on =4.35-4.5 V
   V off =3.9-4.25 V
5. UVP:
   V uvp= 70% Vout
6. OVP:
   V ovp=115%Vout
7. Enable Voltage:
   V rising = 1V
   V falling = 0.4 V
8. Soft start time:
   Tss=2ms
9. Phase selection:
   /X
10. Inrush Current:
    C total = 100 uF
    I inrush= 0.25 A

+3VA_AEC / 100mA

1. Dropout Voltage:
   ⟩ V = 0.21V (Io = 0.3A)
2. OCP:
   I ocp=480mA
3. Short Circuit Current Limit:
   I sc= 320mA
4. Power Dissipation:
   Rthjc =250 /W
   Pd = 0.4W
5. EN Voltage:
   V en = 2V
   V sd =
6. Power OK Voltage:
   Vpokth = 92% *Vout
   Vpokhys = 8%
7. Inrush current:
   T ss = 400uS
   C total =10uF
   I inrush
   R4.5mA
8. FB Voltage:
   VFB = 0.8 V



PM_LEVELDOWN#	CPU_LEVELDOWN	CPU_LEVELDOWN#	Voltage	Status
L	L	H	1.650V	Power Saving
H	L	H	1.795V	Normal
H	H	L	1.927V	Performance
L	H	L	1.782V	N/A

Power stage

1. I/P Current:
   I in = Vo*Io/(0.8 * Vin) =1.175A
2. Ripple Current:
   I rip =1.88A
   I spec=2.5A ⊙1
3. Dynamic:
   I peak=4.7 A
   ESR / 1 pcs =18 mohm
   〉V =84.6mV
4. Inductor Spec:
   I sat=14 A
   I dc =8 A
   DCR=18 mohm
5. MOSFET Spec:

   H-side MOSFET: SI7326DN_T1_E3

   Rds(ON)= 22 mohm (Vgs=4.5 V)
   I cont = 6.5 A (T =25)
   I peak = 40 A (Pause ≦10 us)

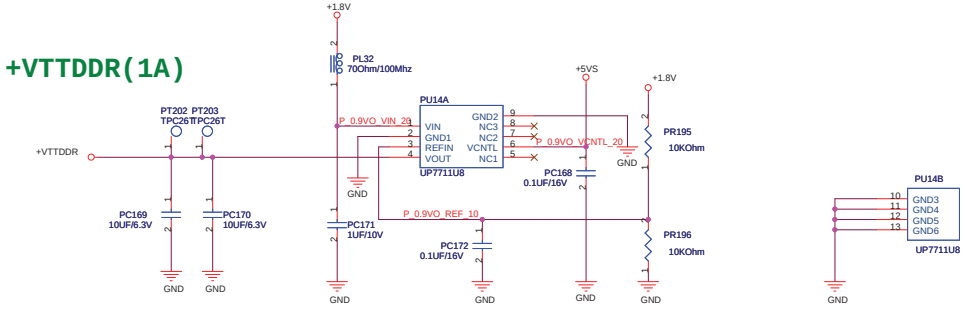
   L-side MOSFET: SI7326DN_T1_E3

   Rds(ON)= 22 mohm (Vgs=4.5 V)
   I cont = 6.5 A (T =25)
   I peak = 40 A (Pause ≦10 us)

Controller

1. Voltage & Current:
   +1.8V@5.8A
2. Frequency:
   PR183=1M ohm
   Fosc=250KHz
3. OCP:
   PR184=10K ohm -> 9A
4. POR:
   Vccrth =3.7~4.1V
   Vcchys=0.2V
5. UVP:
   Vout*70%
6. OVP:
   Vout*115%
7. Enable Voltage:
   V = 2.9V
8. Soft start time:
   Tss=1.2 ms
9. Phase selection:
   /X
10. Inrush Current:
    C total = 100 uF
    I inrush= 0.15 A

+VTTDDR(1A)



+VTTDDR@1 A

1. Dropout Voltage:
   〉V = 0.3V (Io = 2 A)
2. Current Limit:
   I limit = 4 A
3. Continue Current:
   I cont = 3 A
4. Power Dissipation:
   Rthjc = 52 /W
   Pd = 1.9 W
5. EN Voltage:
   V en = 1.4V
   V sd = 0.8 V
6. Supply Voltage:
   Vcc = 5 V
7. Inrush current:
   T ss = 5 ms
   C total = 10 uF
   I inrush = 1.8 mA

<Variant Name>

ASUSTek Computer INC.

Title : +1.8V & +VTTDDR

Engineer: Joy_Zhou

Size	Project Name	Rev
C	1005HA	1.0G

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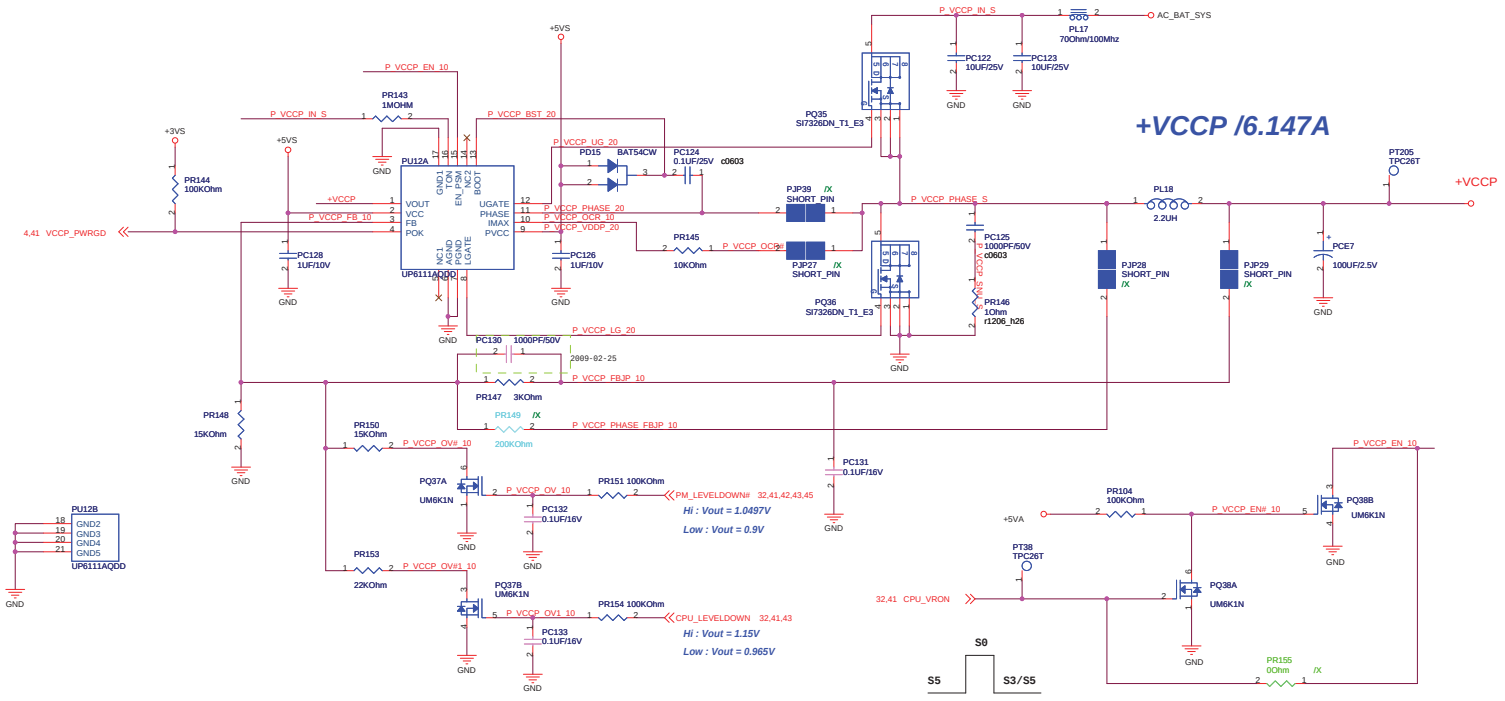

PM_LEVELDOWN#	CPU_LEVELDOWN	CPU_LEVELDOWN#	Voltage	Status
L	L	H	0.9V	Power Saving
H	L	H	1.050V	Normal
H	H	L	1.152V	Performance
L	H	L	1.002V	N/A

Power stage

1. I/P Current:
   I in = Vo*Io/(0.8 * Vin) =0.89A
2. Ripple Current:
   I rip =1.93A
   I spec=2.5A ⊙1
3. Dynamic:
   I peak=6.147 A
   ESR /1 pcs =18 mohm
   〉V =110mV
4. Inductor Spec:
   I sat=14 A
   I dc =8 A
   DCR=18 mohm
5. MOSFET Spec:
   H-side MOSFET: SI7326DN_T1_E3

   Rds(ON)= 22 mohm (Vgs=4.5 V)
   I cont = 6.5 A (T =25)
   I peak = 40 A (Pause ≦10 us)

   L-side MOSFET: SI7326DN_T1_E3

   Rds(ON)= 22 mohm (Vgs=4.5 V)
   I cont = 6.5 A (T =25)
   I peak = 40 A (Pause ≦10 us)

Controller

1. Voltage & Current:
   +VCCP@6.147A
2. Frequency:
   PR143=1.3M ohm
   Fosc=188KHz
3. OCP:
   PR145=10K ohm -> 9A
4. POR:
   Vccrth =3.7~4.1V
   Vcchys=0.2V
5. UVP:
   Vout*70%
6. OVP:
   Vout*115%
7. Enable Voltage:
   V = 2.9V
8. Soft start time:
   Tss=1.2 ms
9. Phase selection:
   /X
10. Inrush Current:
    C total = 100 uF
    I inrush= 0.0875 A

<Variant Name>

ASUSTek Computer INC.	Title : VCCP	
	Engineer: Joy_Zhou	
Size: A2	Project Name: 1005HA	Rev: 1.3G
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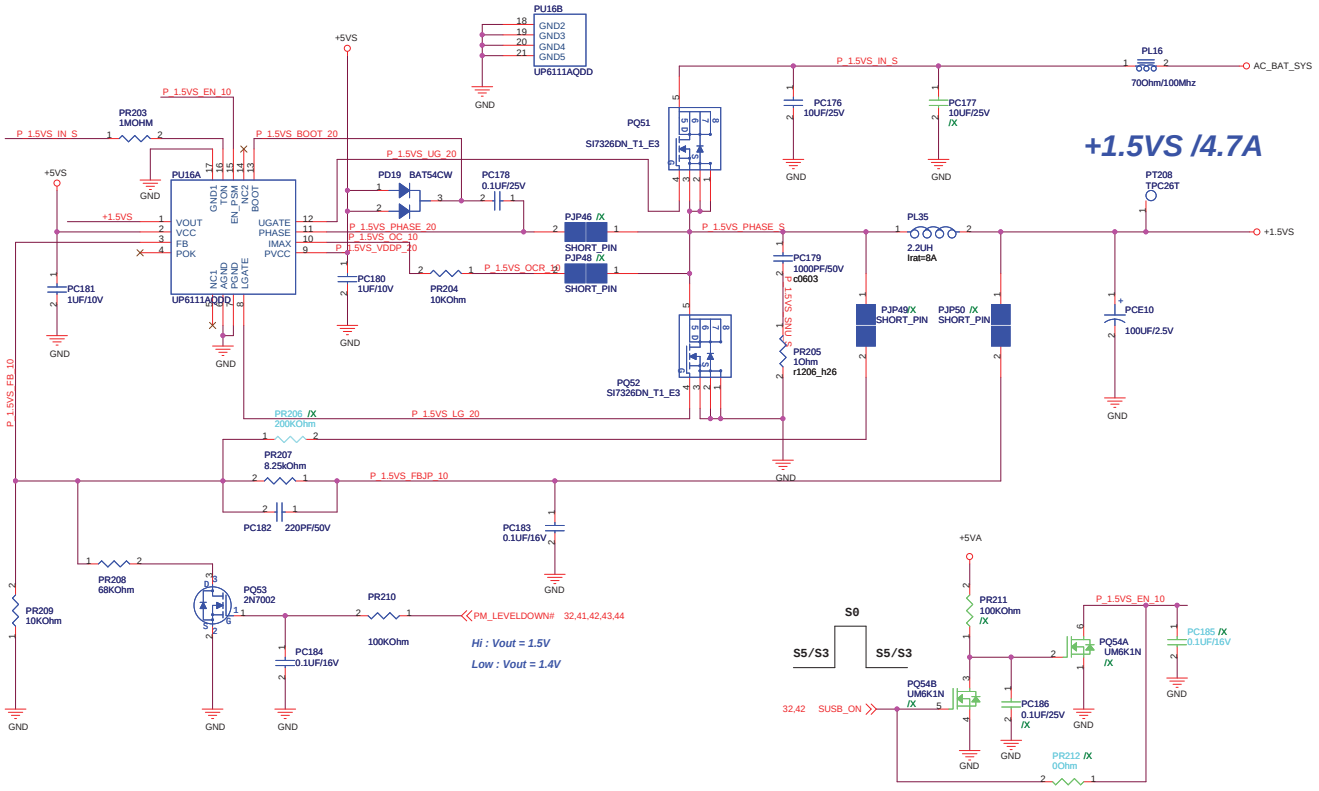
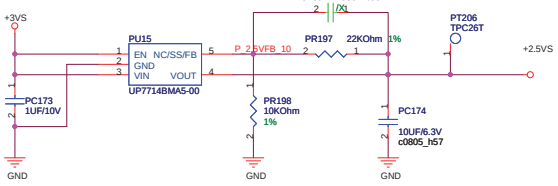




Power stage

1. I/P Current:
   I in = Vo*Io/(0.8 * Vin) =0.83A
2. Ripple Current:
   I rip =1.5A
   I spec=2.5A ⊙1
3. Dynamic:
   I peak=4.7 A
   ESR / 1 pcs =18 mohm
   〉V =84.6mV
4. Inductor Spec:
   I sat=14 A
   I dc =8 A
   DCR=18 mohm
5. MOSFET Spec:

   H-side MOSFET: SI7326DN_T1_E3

   Rds(ON)= 22 mohm (Vgs=4.5 V)
   I cont = 6.5 A (T =25)
   I peak = 40 A (Pause ≦10 us)

   L-side MOSFET: SI7326DN_T1_E3

   Rds(ON)= 22 mohm (Vgs=4.5 V)
   I cont = 6.5 A (T =25)
   I peak = 40 A (Pause ≦10 us)

Controller

1. Voltage & Current:
   +1.5VS@4.7A
2. Frequency:
   PR203=1M ohm
   Fosc=250KHz
3. OCP:
   PR204=10K ohm -> 9A
4. POR:
   Vccrth =3.7~4.1V
   Vcchys=0.2V
5. UVP:
   Vout*70%
6. OVP:
   Vout*115%
7. Enable Voltage:
   V = 2.9V
8. Soft start time:
   Tss=1.2 ms
9. Phase selection:
   /X
10. Inrush Current:
    C total = 100 uF
    I inrush= 0.125 A

<Variant Name>

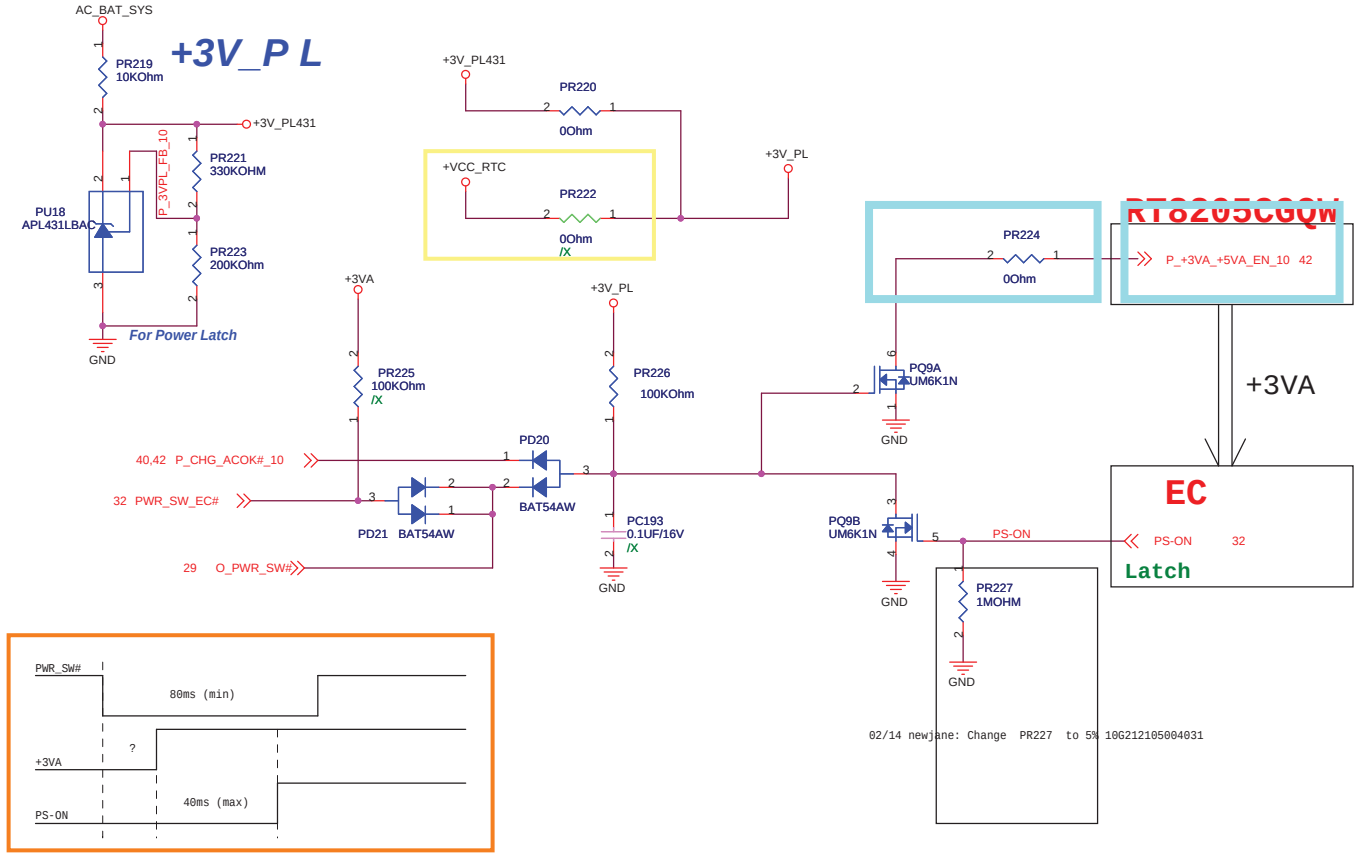
ASUSTek Computer INC.

Title : +1.5VS & +2.5VS

Engineer: Joy_Zhou

Size	Project Name	Rev
C	1005HA	1.0G

Date: Thursday, March 19, 2009 Sheet 45 of 48



Title	<Title>		
Size A3	Document Number <Doc>		Rev <RevCode>
Date: Thursday, March 19, 2009		Sheet 46 of 48	

Ver	Descrption	Date
1.0G	change UF1 to the same as 1005hn's	2009.0122.2027
	change lvds conn P/N to 12G170190201 change CPU P/N from 01G012290000 to 01G012520100 P4:糟 CC50 ..CC57 豔篆臂ㄒ clock gen pin 狠 P23:糟 GC21 P29: 奔IL2	2009.0203.1555
	update NB symbol 癸clock gen ㎝ WIFI 场だ 酚1005HN 秈≯ 穗	2009.0205.1555
	P4: C_PCIE_LAN_R C_PCIE_LAN#_R H_ITP_CKOUT H_ITP_CKOUT# add 10pf for RF P23: cancel BL_EN, G_LVDD_EN, G_NBL_CTRL EMI cap	2009.0205.2120
	ADD LR55 02/14 newjane: Change PR227 to 5% 10G212105004031 02/14 newjane: Change OR1 from 18.2K to 18K 10G212180214010 02/14 newjane: Change HR1 from 68ohm to 56 ohm 02/14 newjane: Change SR1 from 20K 10G2122002141l0to 20K 10G212200214030 02/14 newjane: ChangeHC18 from 11G23211021115 to 11G232110214030 02/14 newjane: ChangeHC6 GC20 HC11 HC12 from 11G233310531360 to11G233210516320 02/14 newjane: /X LC41 02/14 newjane: SD RC1 RC7 RC12 from 11G2323104313601o11G232110411320 02/14 xiao-jie SR4 PR227 from 10G212105004031 to 10G212100414030 02/14 xiao-jie aAR8 AR5 from 10G212200214110 to 10G212200214030 02/14 xiao-jie AR7 P/N toPR105 P/N	2009.0210.1513

Title : <Title>		
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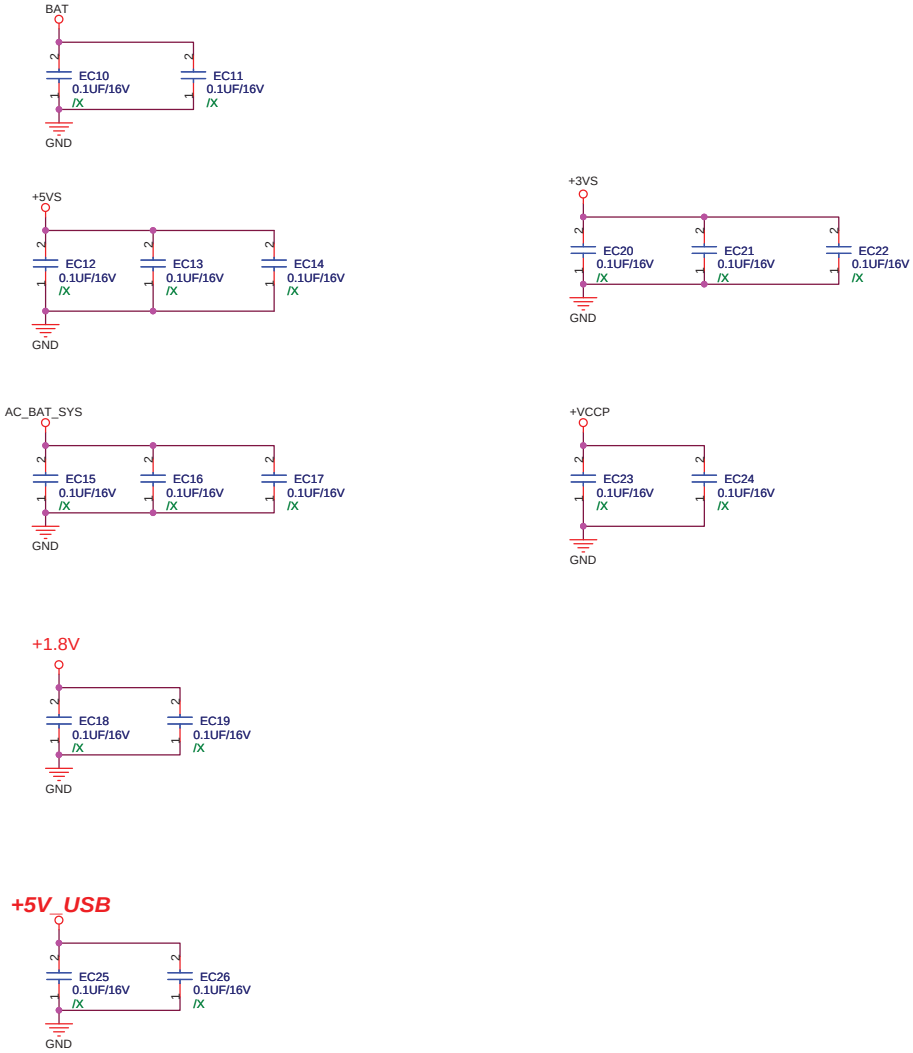

<OrgName>	Title : <Title>	
	Engineer: Lus Lu	
Size: A3	Project Name: <Doc>	Rev: 1.0
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