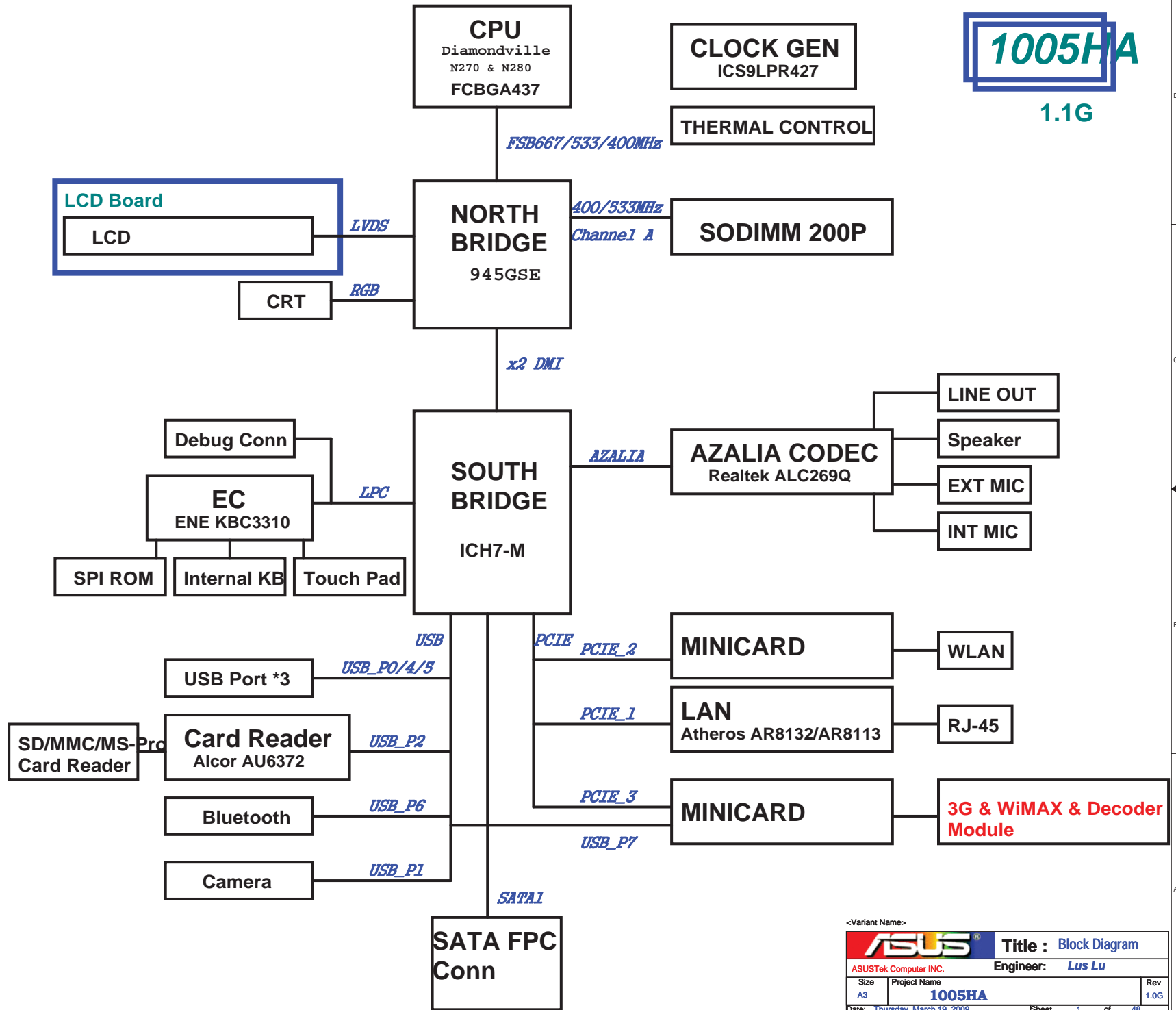


- 01_Block Diagram
- 02_System Setting
- 03_Power Sequence
- 04_Clock Gen_ICS9LPR434
- 05_Diamondville_BUS
- 06_Diamondville_PWR
- 07_NB-945GMS(HOST)
- 08_NB-945GMS(DMI)
- 09_NB-945GMS(GRAPHIC)
- 10_NB-945GMS(DDR2)
- 11_NB-945GMS(PWR)
- 12_NB-945GMS(PWR2)
- 13_NB-945GMS(GND)
- 14_SB-ICH7M(PWR)
- 15_SB-ICH7M(1)
- 16_SB-ICH7M(2)
- 17_SB-ICH7M(3)
- 18_DDR2 SODIMM
- 19_DDR2 Termination
- 20_Onboard VGA
- 21_LCD Conn_LID
- 22_Blank
- 23_Mini WIFI+ BT
- 24_LAN_Atheros AR8113
- 25_RJ45
- 26_Flash Conn
- 27_USB Port
- 28_Camera Conn
- 29_Card Reader_AU6372A51
- 30_Codec_ALC269
- 31_Audio_AMP_Jack
- 32_EC_ENE KB3310
- 33_EC
- 34_Switch_SPI ROM_Debug Conn
- 35_Thermal Sensor_FAN
- 36_KB_Touch Pad
- 37_LED_THERMTRIP
- 38_Discharge
- 39_PWR Jack
- 40_Srew Hole
- 41_EMI
- 42_POWER FLOW
- 43_Vcore
- 44_Power System
- 45_Power_+1.8V & VTTDDR
- 46_Power_VCCP
- 47_Power_+1.5VS & +2.5VS
- 48_Power_Charger
- 49_EC Pin Define
- 49_History



1005HA

1.1G

EEE PC 701 PCB version

GPI37	GPI38	GPI39	PCB version
0	0	0	
0	0	0	
0	0	1	
0	0	1	
0	1	0	
0	1	0	
0	1	1	
0	1	1	
1	0	0	
1	0	0	
1	0	1	
1	0	1	
1	1	0	
1	1	0	
1	1	1	
1	1	1	

USB

USB 0	NC
USB 1	USB Conn
USB 2	USB Conn
USB 3	USB Conn
USB 4	Card Reader
USB 5	Minicard
USB 6	Bluetooth
USB 7	Camera

PCIE

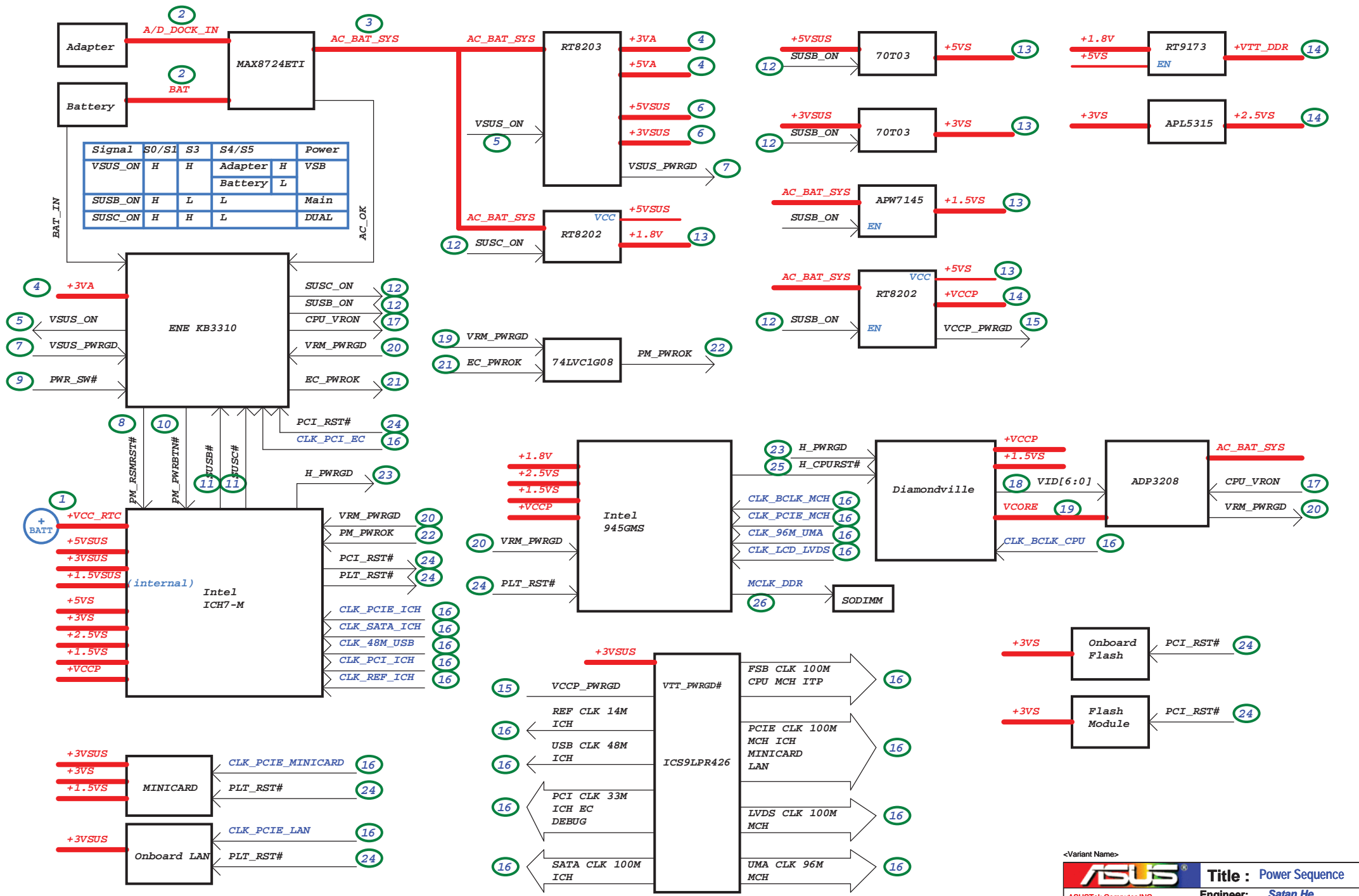
PCIE 1	NC
PCIE 2	LAN
PCIE 3	Minicard
PCIE 4	SSD

Azalia

ACZ_SDIN0	CODEC
ACZ_SDIN1	NC
ACZ_SDIN2	NC

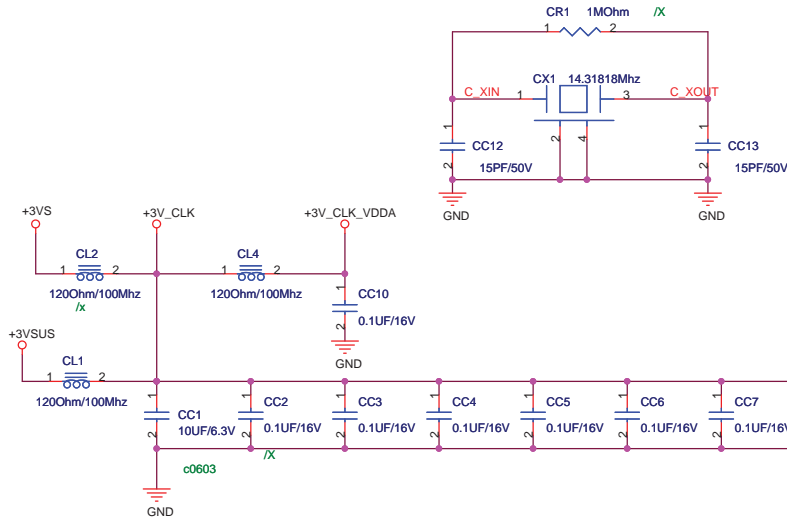
<Variant Name>

		Title : System Setting	
ASUSTek Computer INC.		Engineer: Satan_He	
Size A3	Project Name 1005HA	Rev 1.0G	
Date: Thursday, March 19, 2009		Sheet 2 of 48	



Signal	S0/S1	S3	S4/S5	Power
VSUS_ON	H	H	Adapter Battery	H L
SUSB_ON	H	L	L	Main
SUSC_ON	H	H	L	DUAL

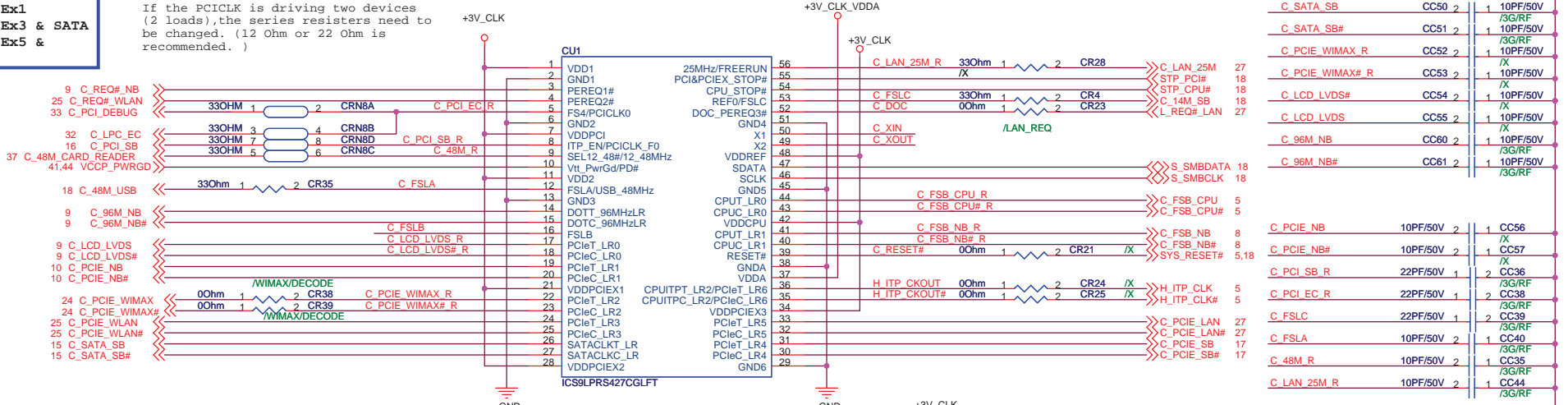
<< C_14M_SB	18	<< STP_PCI#	18
<< S_SMBDATA	18	<< STP_CPU#	18
<< C_FSB_CPU	5	<< C_PCI_DEBUG	33
<< C_FSB_CPU#	5	<< C_LPC_EC	32
<< C_FSB_NB	8	<< C_PCI_SB	16
<< C_FSB_NB#	8	<< C_48M_CARD_READER	37
<< H_ITP_CLK	5	<< C_48M_USB	18
<< H_ITP_CLK#	5	<< C_96M_NB	9
<< C_PCIE_WLAN#	25	<< C_96M_NB#	9
<< C_PCIE_WLAN	25	<< C_LCD_LVDS	9
<< SYS_RESET#	5,18	<< C_LCD_LVDS#	9
<< C_REQ#_NB	9	<< C_PCIE_NB#	10
<< C_PCIE_NB	10	<< C_PCIE_NB	10
<< C_REQ#_WLAN	25	<< C_PCIE_SB	17
<< BSEL0	6	<< C_PCIE_SB#	17
<< C_LAN_25M	27	<< C_PCIE_LAN	27
<< VCCP_PWRGD	41,44	<< C_PCIE_LAN#	27



1:Disable
0:Enable

PEREQ1:PCIEx0 & PCIEx1
PEREQ2:PCIEx2 & PCIEx3 & SATA
PEREQ3:PCIEx4 & PCIEx5 & PCIEx6

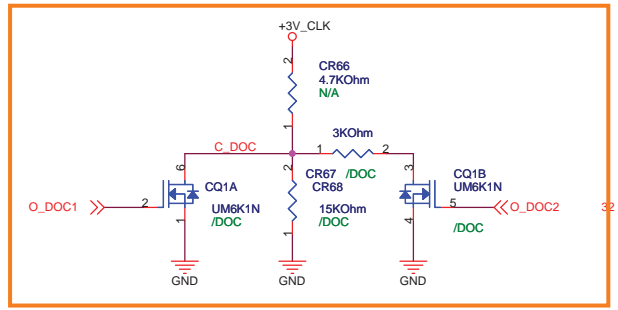
If the PCICLK is driving two devices (2 loads), the series resistors need to be changed. (12 Ohm or 22 Ohm is recommended.)



O_DOC1	O_DOC2	Voltage	Status
L	L	2.0-3.3V	Super
L	H	0.7-1.5V	Normal
H	*	0V	Power saving

FSLQ	FSLB	FSLA	CPU(MHZ)
0	0	1	133.33
0	1	1	166

CLK_FSLC	Strapping Define
1.8V-3.3V	enter Test Mode
0.7V-1.8V	FSB trap High
0V-0.35V	FSB trap Low



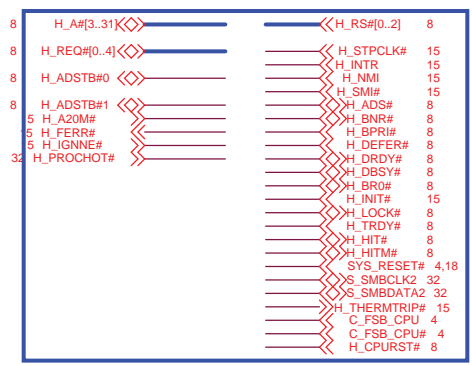
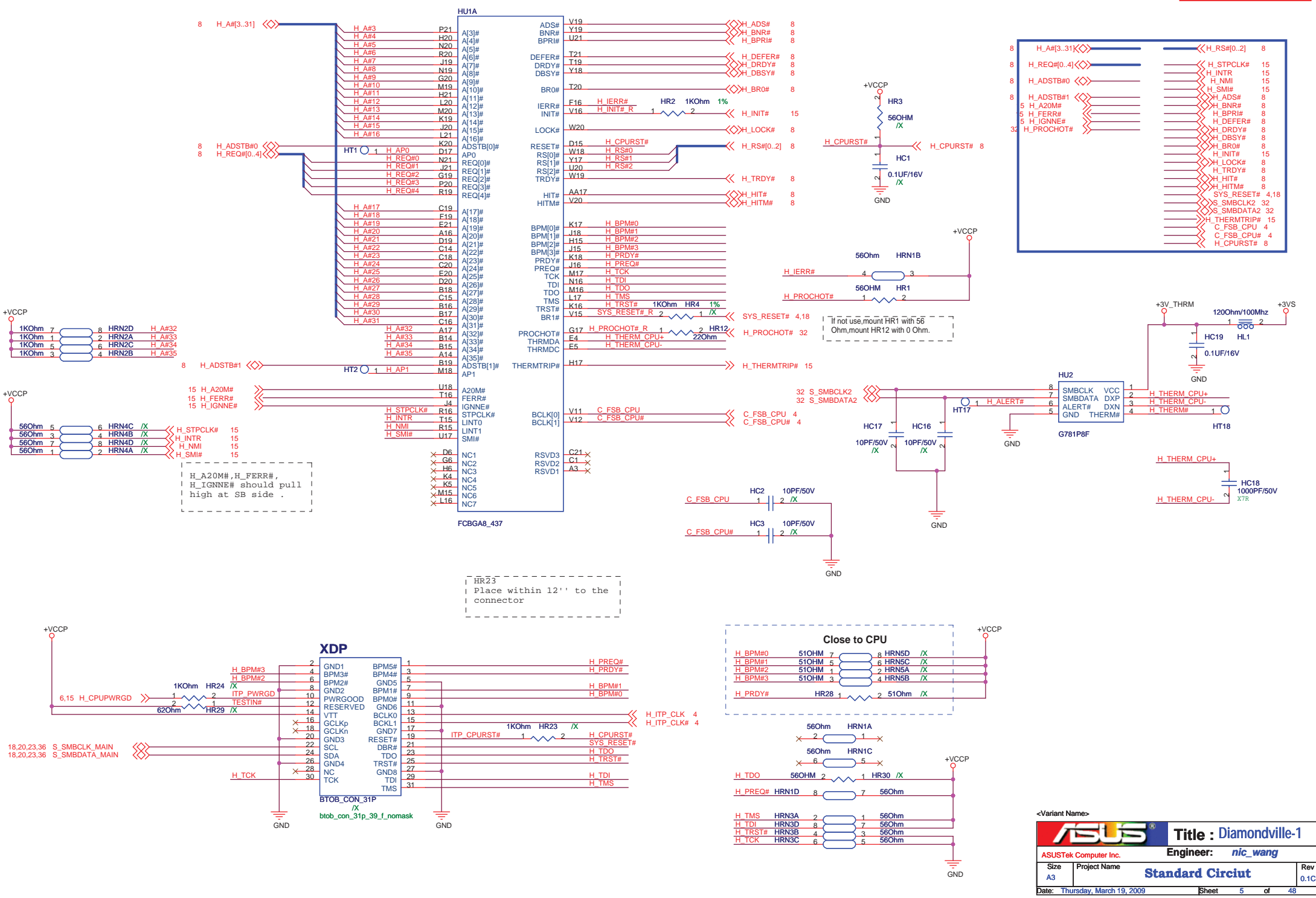
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ASUS Title : Clock Gen_ICS9LPR427

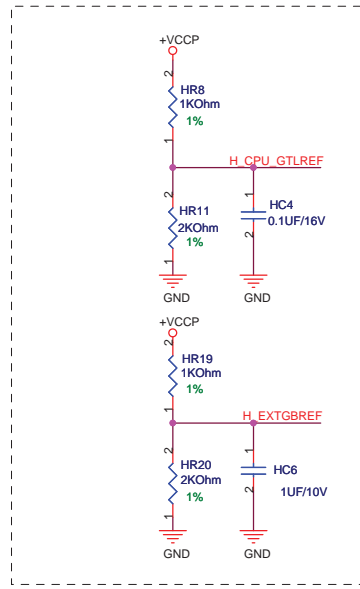
ASUSTek Computer INC. Engineer: nic_wang

Size	Project Name	Rev
A3	standard circuit	0.1B

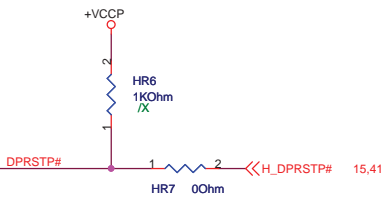
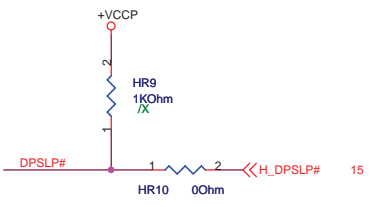
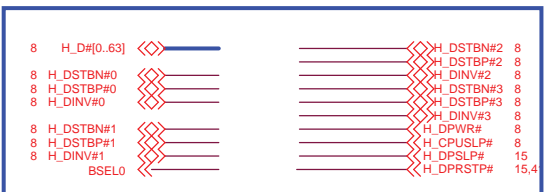
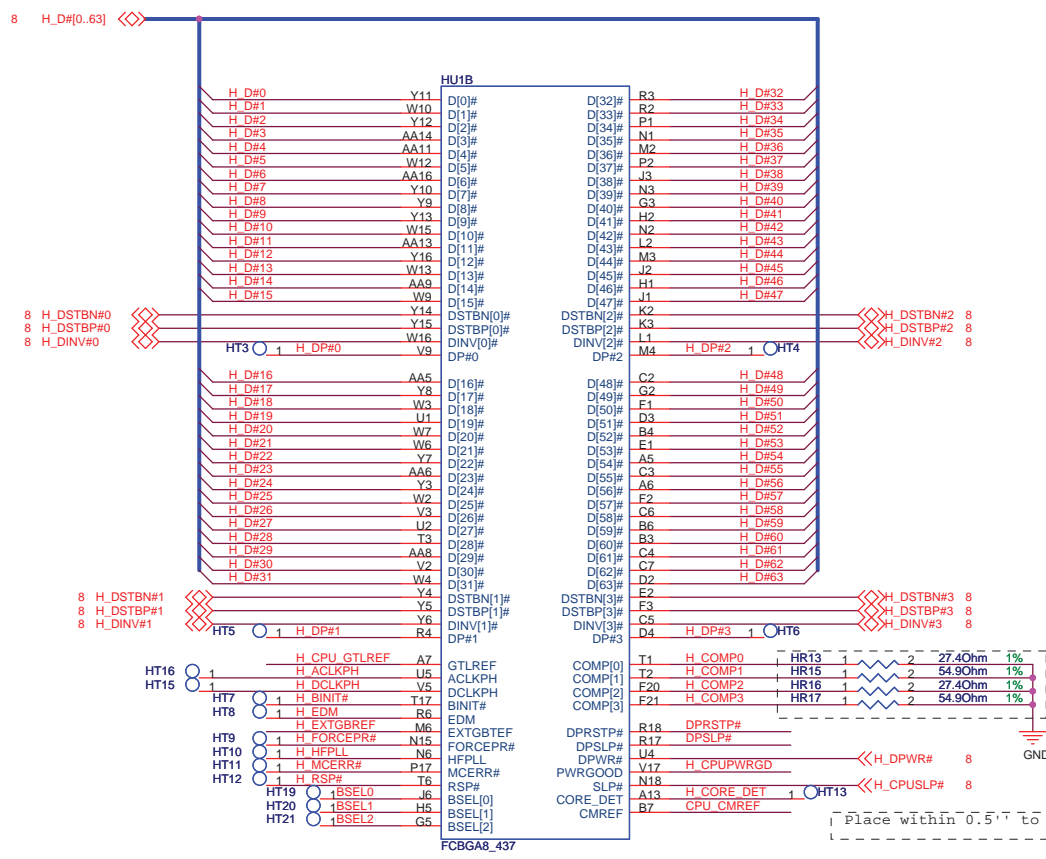
Date: Thursday, March 19, 2009 Sheet 4 of 48



Place within 0.5" to processor pin

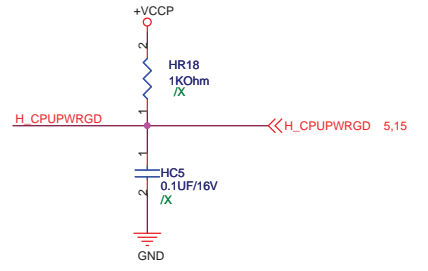
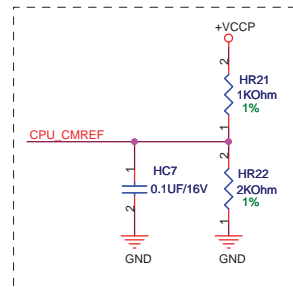
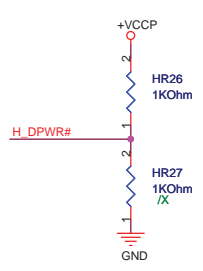


BSEL0	BSEL1	BSEL2	FSB
0	X	X	400
1	X	X	533



Γ H_DPRSTP#cmH_DPUSLP# 0
 Ohm=,い 1KOhm Pull
 up, ,い, 惠 1 KOhm Pull
 up, (紘))ノ p0ohm 奔 锁 碇

Place within 0.5" to processor pin



Place within 0.5" to processor pin

H_PWRGD-->H_CPUPWRGD

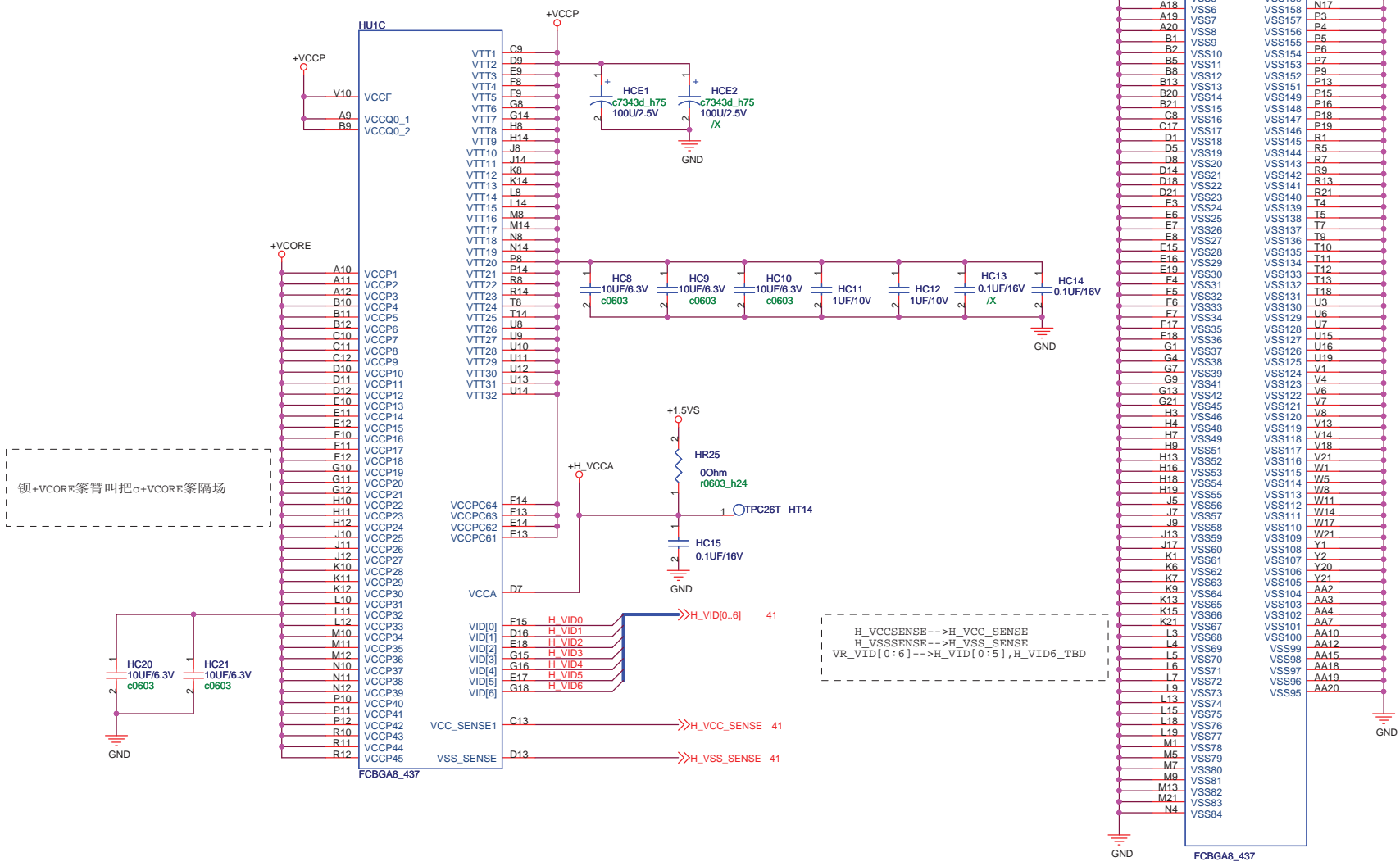
<Variant Name>

Title : Diamondville-2

ASUSTek Computer Inc. **Engineer:** nic_wang

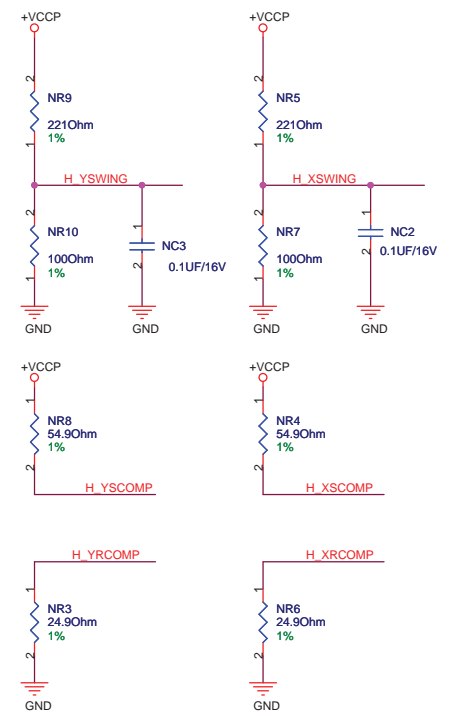
Size	Project Name	Rev
A3	Standard Circuit	0.1C

Date: Thursday, March 19, 2009 Sheet 6 of 48



锁+VCCO0_1禁替叫把+VCCO0_2禁隔场

H_VCCSENSE-->H_VCC_SENSE
H_VSSSENSE-->H_VSS_SENSE
VR_VID[0:6]-->H_VID[0:5],H_VID6_TBD



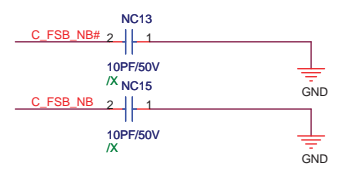
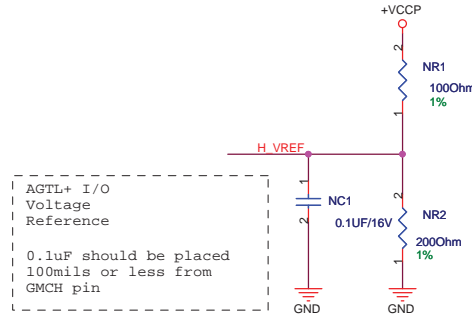
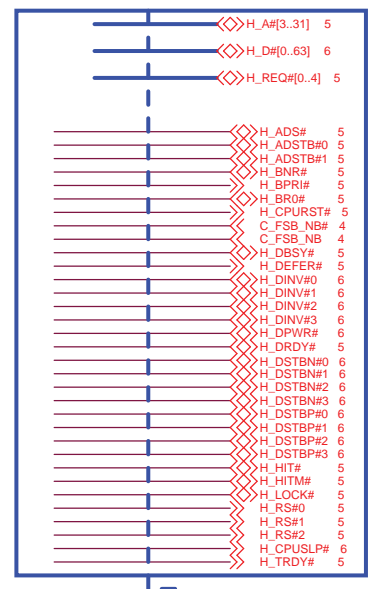
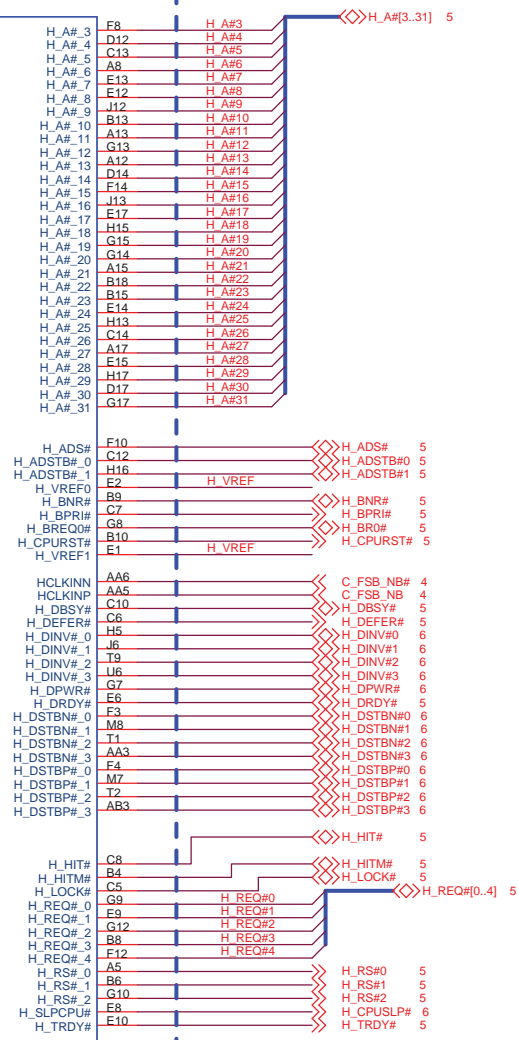
Voltage Swing
For Providing a Reference Voltage to the FSB RCOMP circuit
Signal voltage level=
 $0.3125 * V_{CCP}$
Trace should be 10 mil wide with 20 mil spacing

SCOMP
For Slew Rate Compensation on the FSB

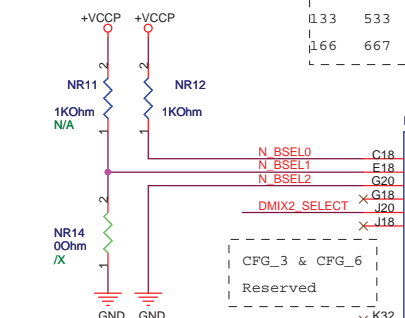
RCOMP
For Calibrating the FSB I/O Buffer

H_D#0	C4	H_D#_0
H_D#1	F6	H_D#_1
H_D#2	H9	H_D#_2
H_D#3	H6	H_D#_3
H_D#4	F7	H_D#_4
H_D#5	E3	H_D#_5
H_D#6	C2	H_D#_6
H_D#7	C3	H_D#_7
H_D#8	K9	H_D#_8
H_D#9	F5	H_D#_9
H_D#10	J7	H_D#_10
H_D#11	K7	H_D#_11
H_D#12	H8	H_D#_12
H_D#13	E5	H_D#_13
H_D#14	K8	H_D#_14
H_D#15	J8	H_D#_15
H_D#16	J2	H_D#_16
H_D#17	J3	H_D#_17
H_D#18	N1	H_D#_18
H_D#19	M5	H_D#_19
H_D#20	K5	H_D#_20
H_D#21	J5	H_D#_21
H_D#22	H3	H_D#_22
H_D#23	J4	H_D#_23
H_D#24	N3	H_D#_24
H_D#25	M4	H_D#_25
H_D#26	M3	H_D#_26
H_D#27	N8	H_D#_27
H_D#28	N6	H_D#_28
H_D#29	K3	H_D#_29
H_D#30	N9	H_D#_30
H_D#31	M1	H_D#_31
H_D#32	V8	H_D#_32
H_D#33	V9	H_D#_33
H_D#34	R6	H_D#_34
H_D#35	T8	H_D#_35
H_D#36	R2	H_D#_36
H_D#37	N5	H_D#_37
H_D#38	N2	H_D#_38
H_D#39	R5	H_D#_39
H_D#40	U7	H_D#_40
H_D#41	R8	H_D#_41
H_D#42	T4	H_D#_42
H_D#43	T7	H_D#_43
H_D#44	R3	H_D#_44
H_D#45	T5	H_D#_45
H_D#46	V6	H_D#_46
H_D#47	V3	H_D#_47
H_D#48	W2	H_D#_48
H_D#49	W1	H_D#_49
H_D#50	V2	H_D#_50
H_D#51	W4	H_D#_51
H_D#52	W7	H_D#_52
H_D#53	W5	H_D#_53
H_D#54	V5	H_D#_54
H_D#55	AB4	H_D#_55
H_D#56	AB8	H_D#_56
H_D#57	W8	H_D#_57
H_D#58	AA9	H_D#_58
H_D#59	AA8	H_D#_59
H_D#60	AB1	H_D#_60
H_D#61	AB7	H_D#_61
H_D#62	AA2	H_D#_62
H_D#63	AB5	H_D#_63

HOST

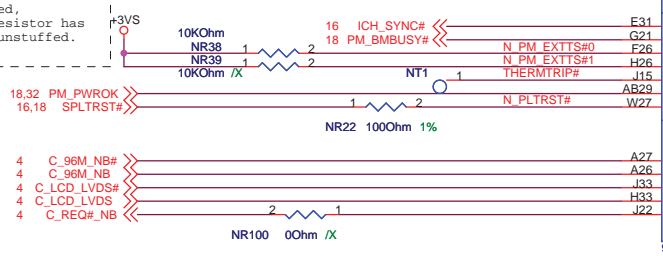


BCLK	FSB	BSEL2	BSEL1	BSEL0
133	533	L	L	H
166	667	L	H	H

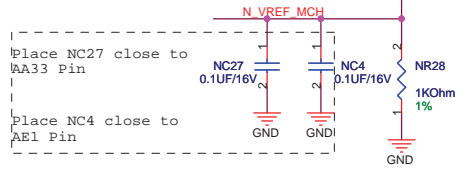
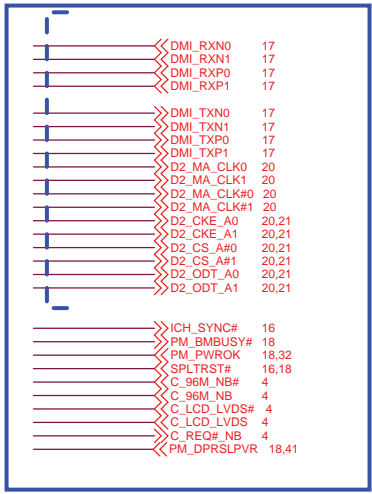
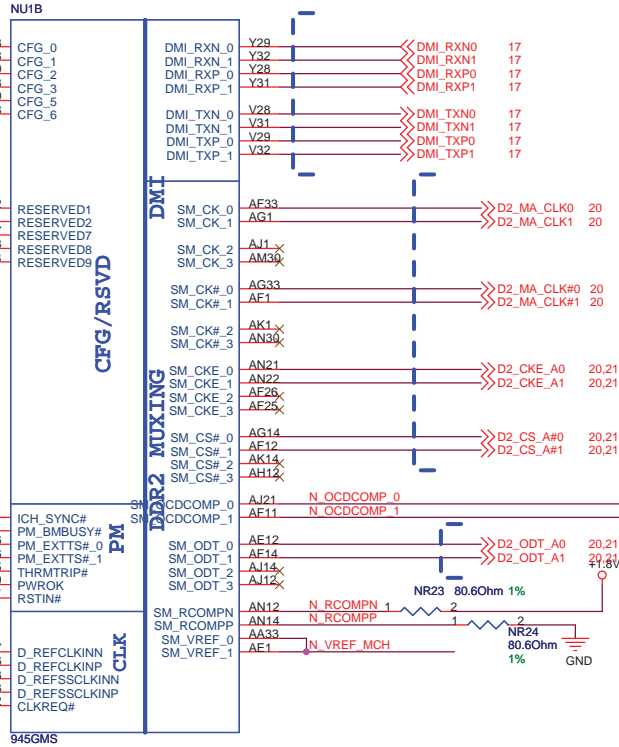


DMIX2_SELECT
0=DMI X2 (DEFAULT)
1=Reserved

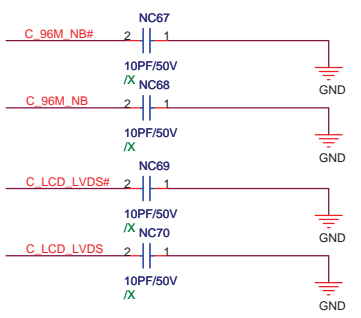
A 10K-Ohm pull up resistor has been used on the PM_EXTTS#_1, if the Fast C4E feature is required, this resistor has to be unstuffed.

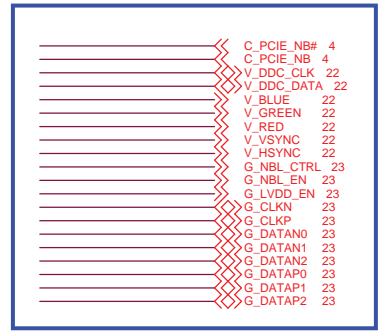
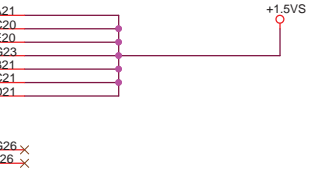
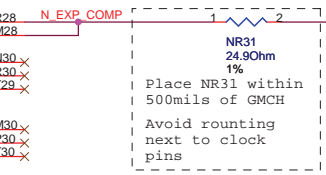
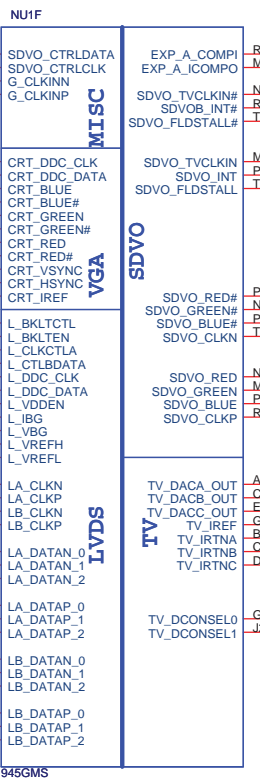
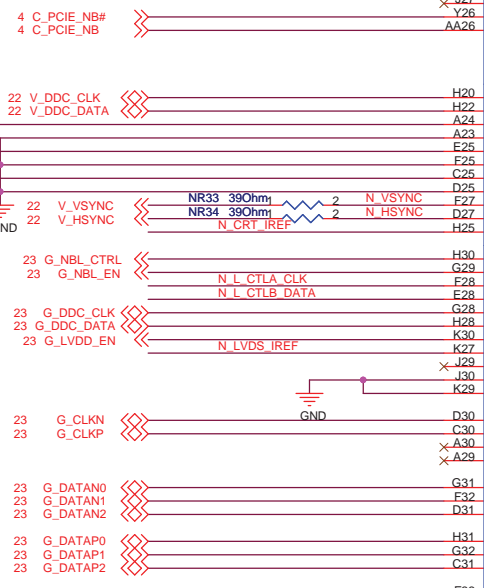
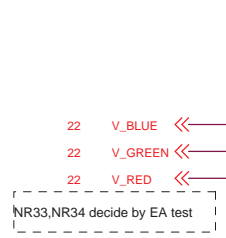
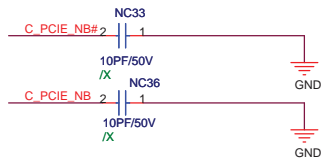
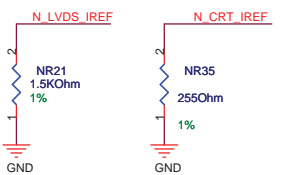
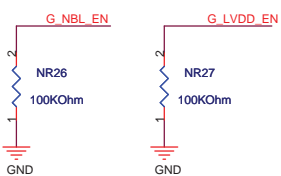
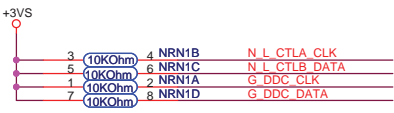
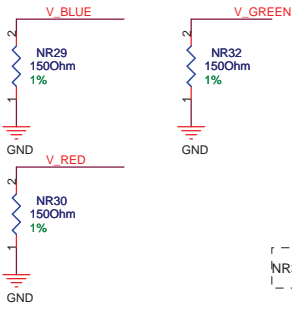
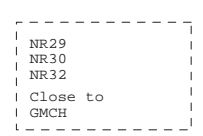


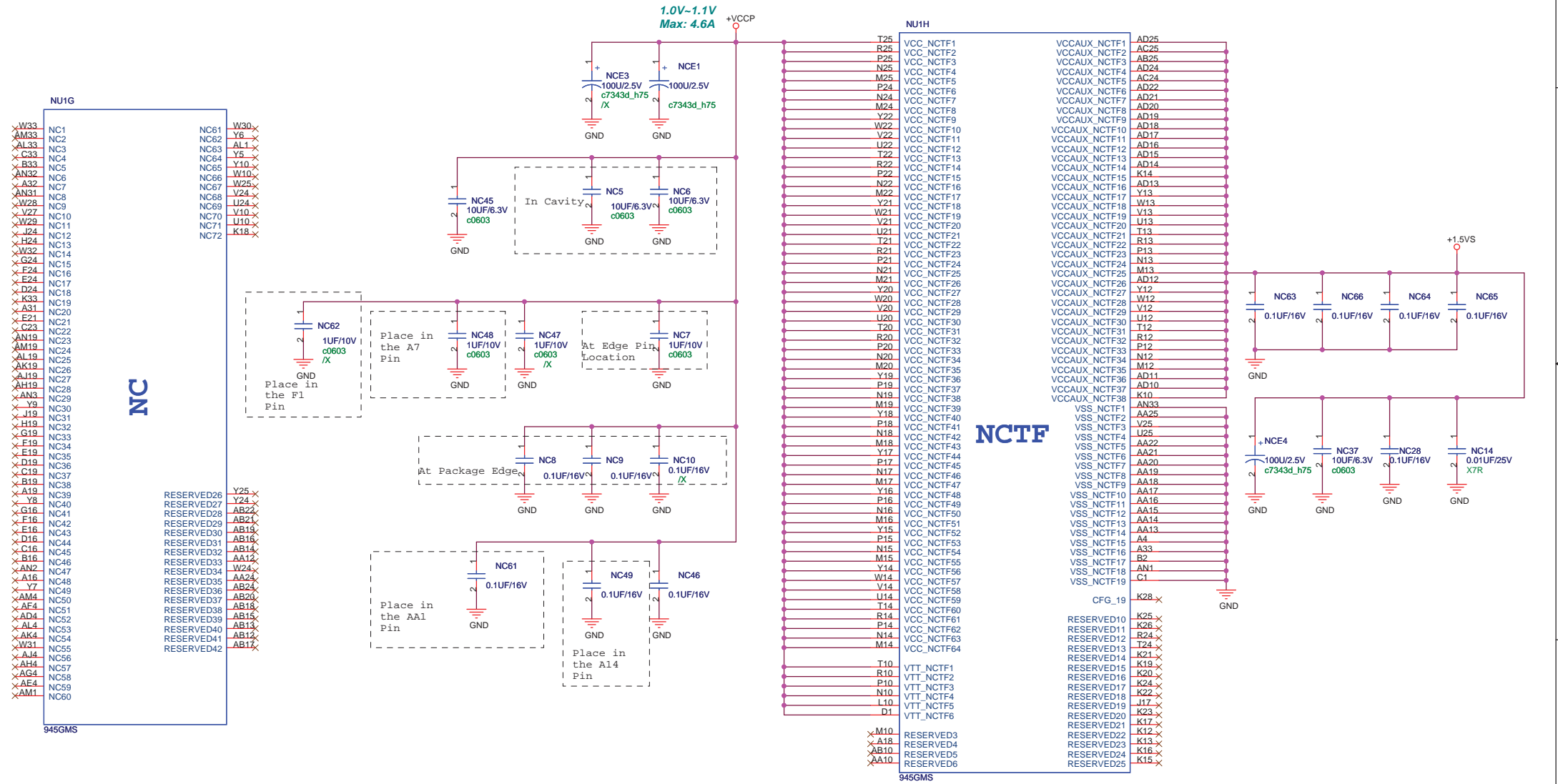
N_PM_EXTTS#1
0.1C Bate
EXTTS1# can alternately be used to implement fast C4/C4E exit, IF the Fast C4E feature is required, PM_EXTTS1# have to connect to DPRSLPVR

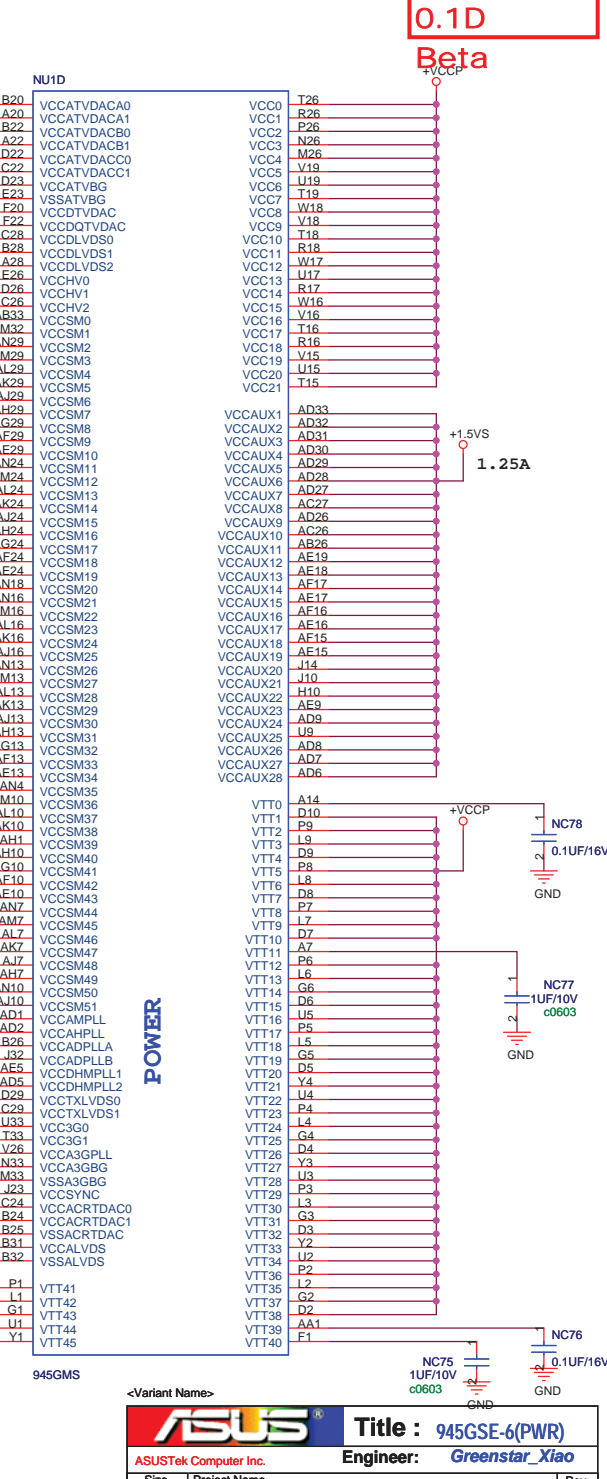
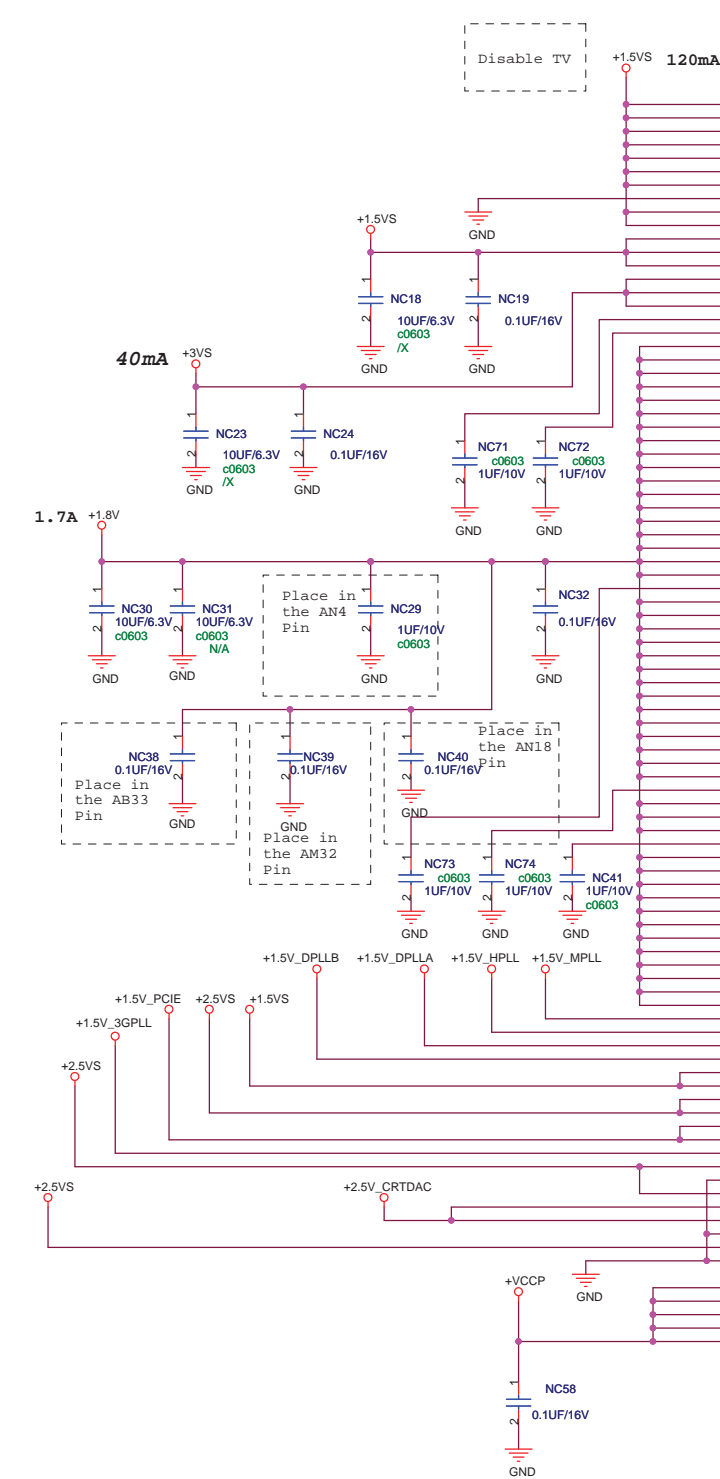
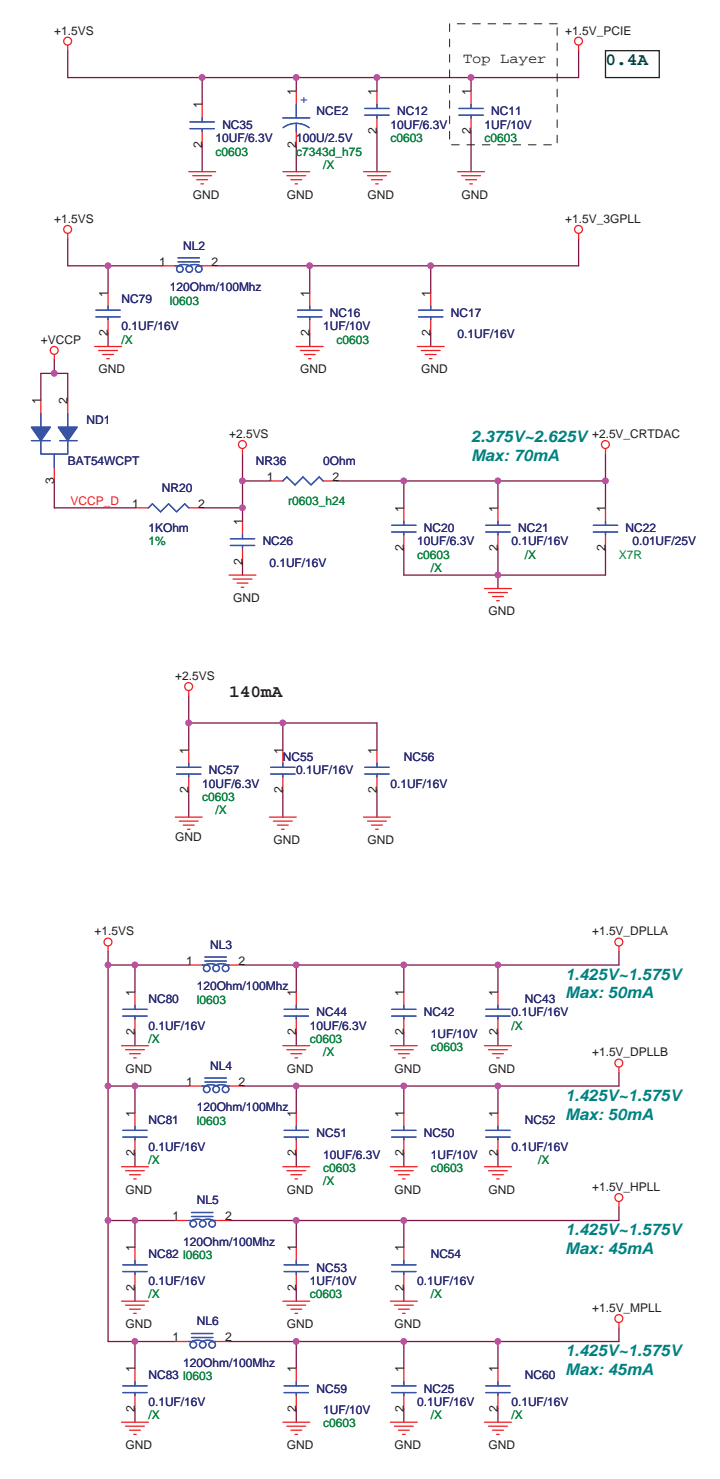


Place NC27 close to A33 Pin
Place NC4 close to A61 Pin





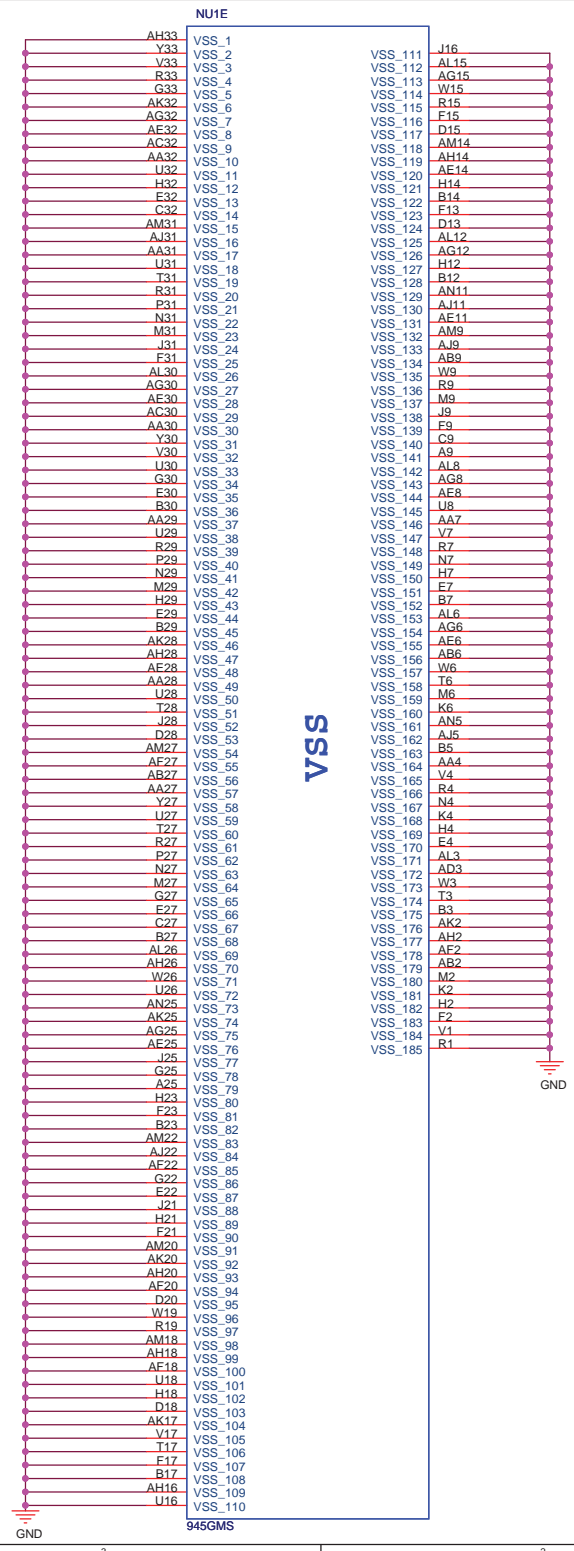




ASUS Title: 945GSE-6(PWR)
 ASUSTek Computer Inc. Engineer: Greenstar_Xiao

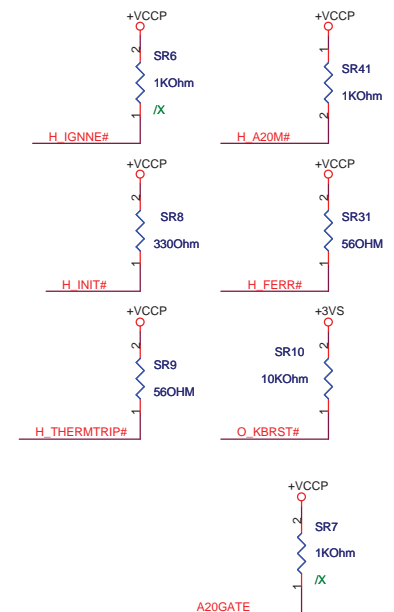
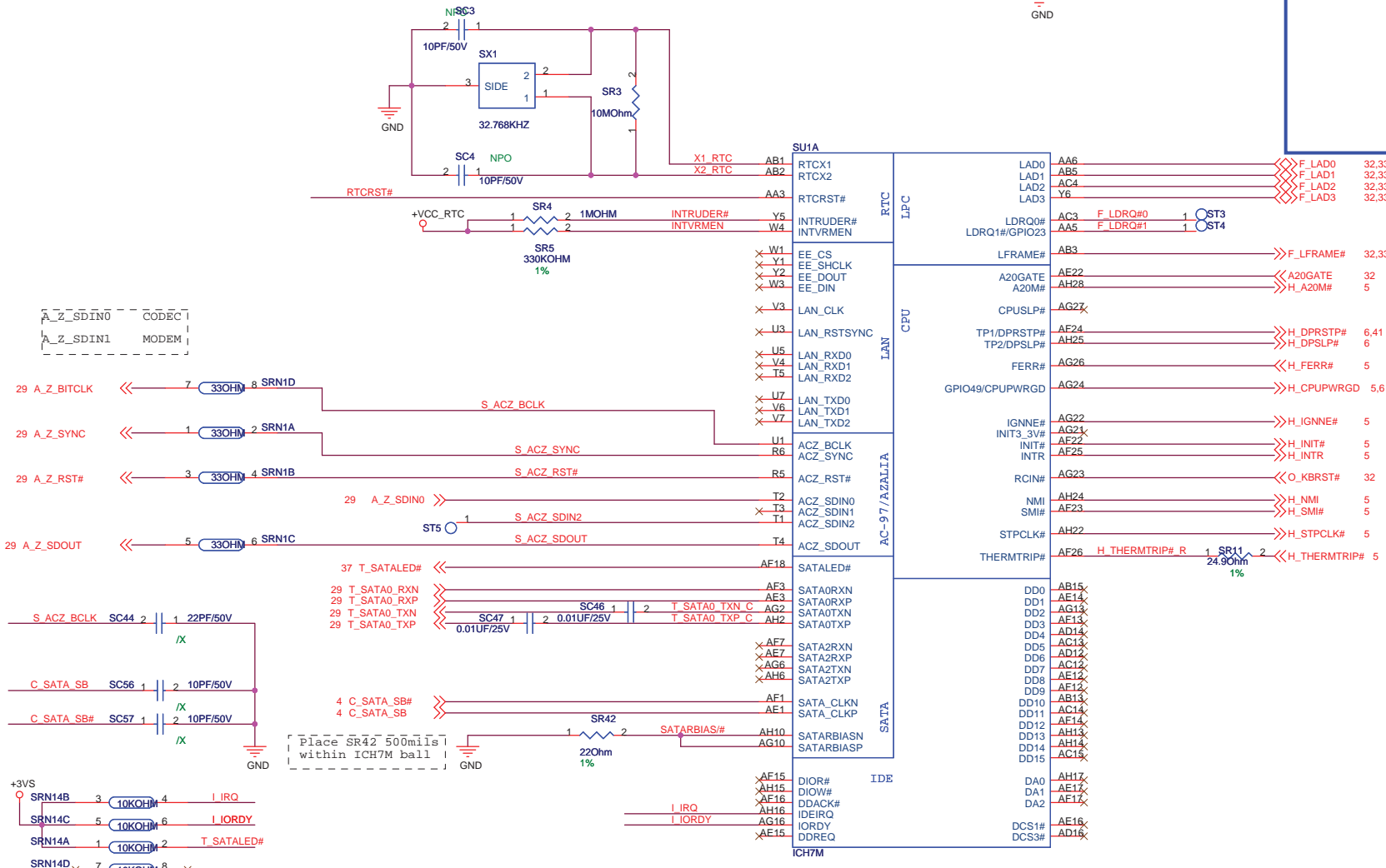
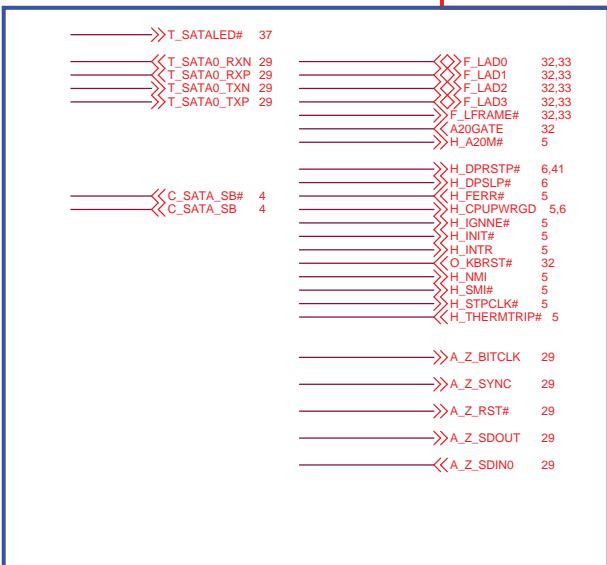
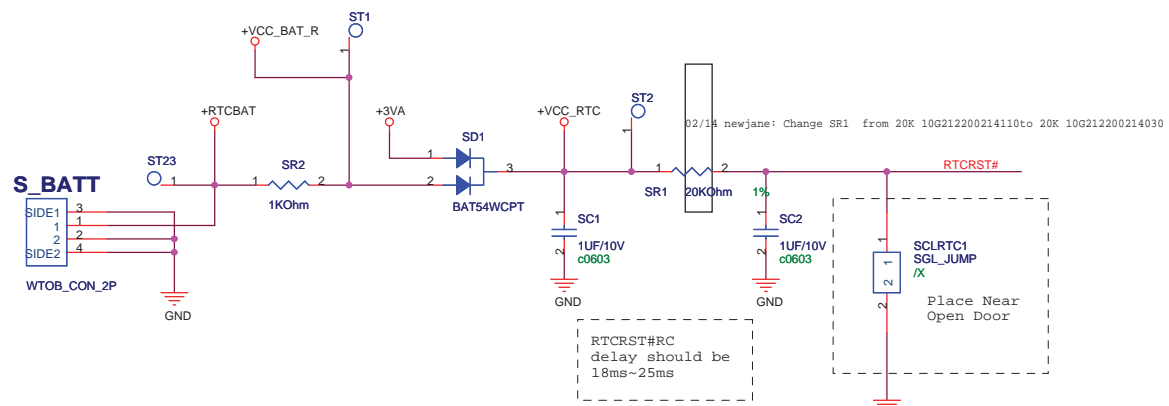
Size	Project Name	Rev
A3	Standard Circuit	0.1D

Date: Thursday, March 19, 2009 Sheet 13 of 48



<Variant Name>

		Title : 945GSE-7(GND)	
ASUSTek Computer Inc.		Engineer: Greenstar_Xiao	
Size	Project Name	Rev	
A3	Standard Circuit	0.1D	
Date: Thursday, March 19, 2009			
Sheet		14	of 48

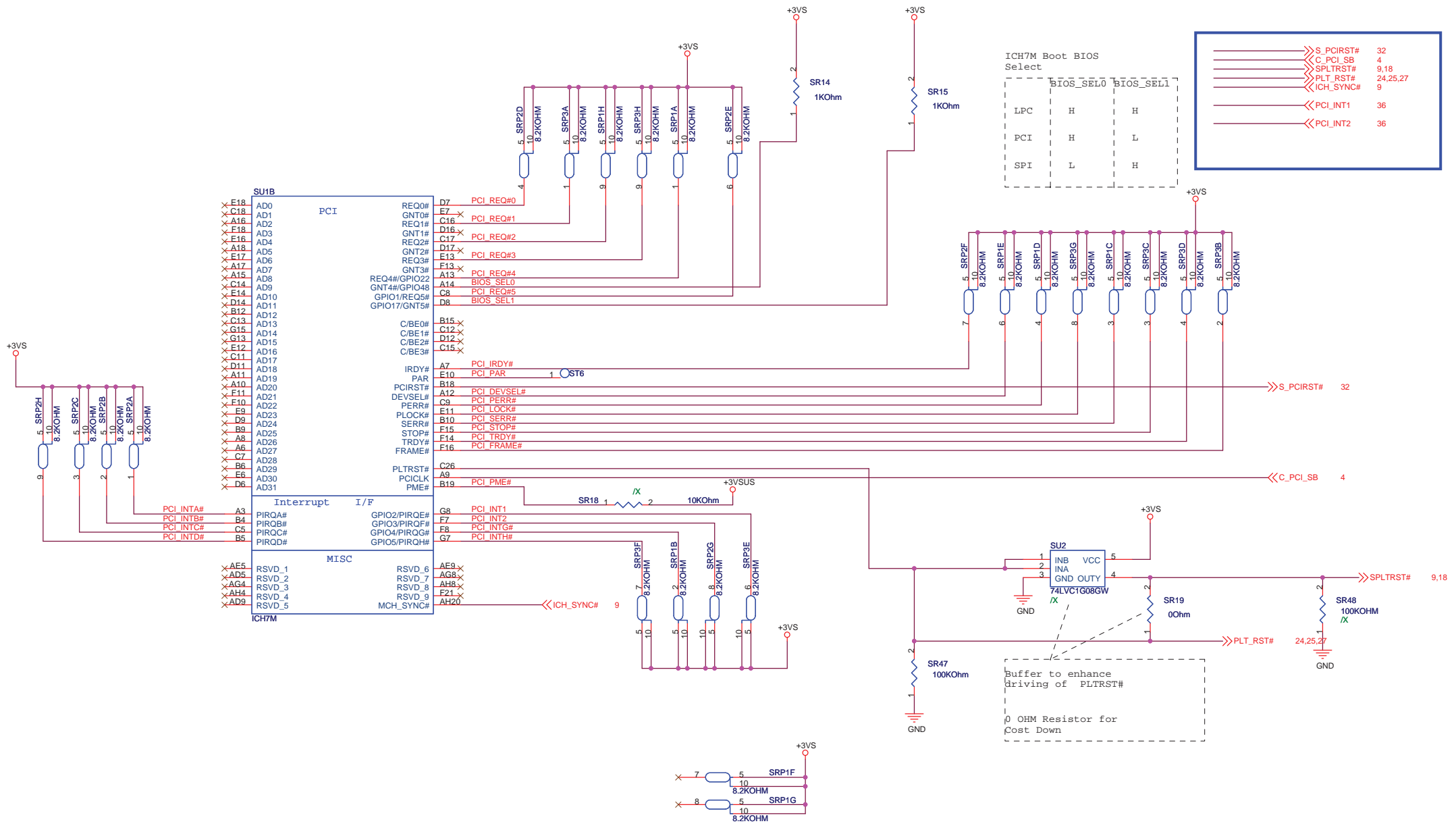


<Varient Name>

Title : ICH7M-1
Engineer: Endy_Wu

Size	Project Name	Rev
A3	Standard Circuit	0.1B

Date: Thursday, March 19, 2009 Sheet 15 of 48




ICH7M Boot BIOS Select

BIOS_SEL0	H	H
PCI	H	L
SPI	L	H

→ S_PCIRST#	32
→ C_PCI_SB	4
→ SPLTRST#	9,18
→ PLT_RST#	24,25,27
→ ICH_SYNC#	9
← PCI_INT1	36
← PCI_INT2	36

Buffer to enhance driving of PLTRST#
0 OHM Resistor for Cost Down

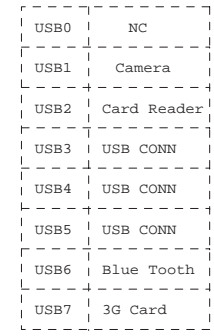
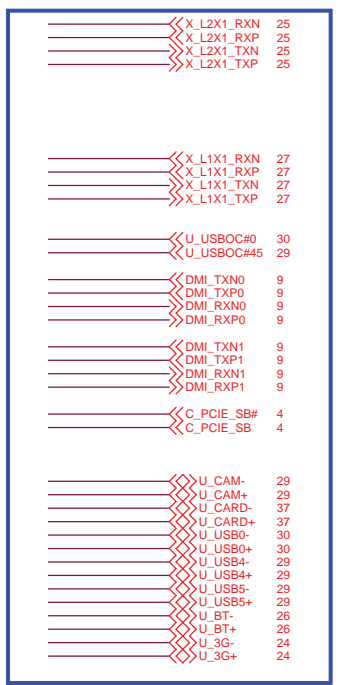
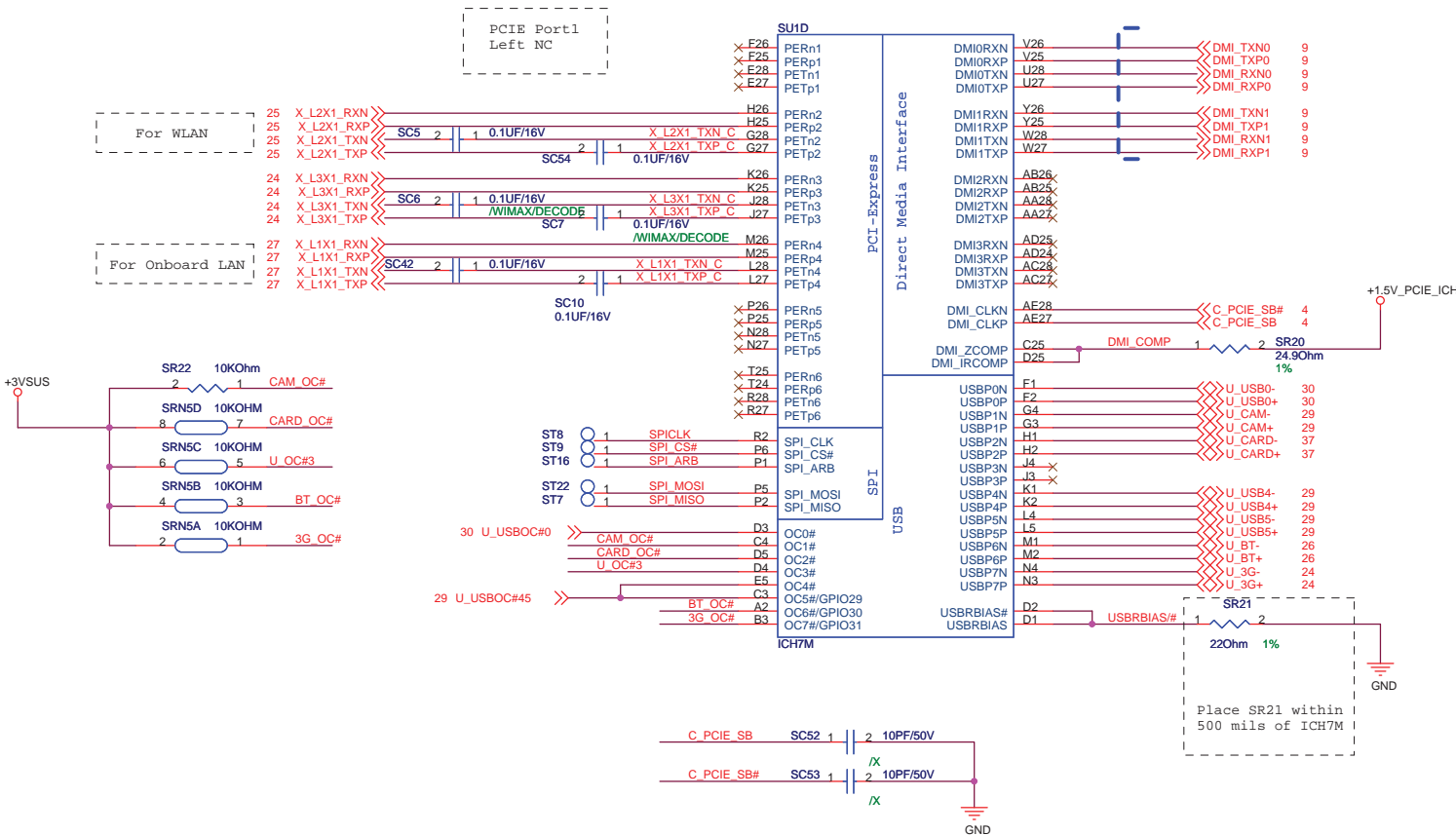
<Variant Name>

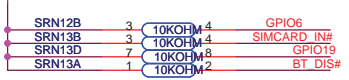
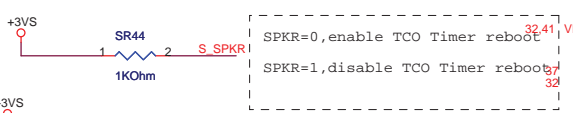
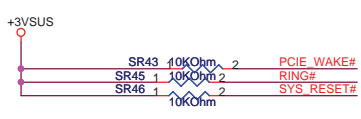
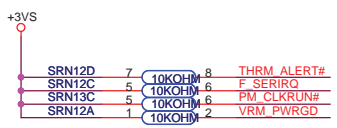
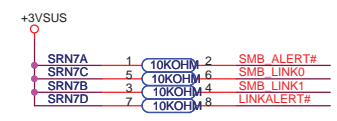
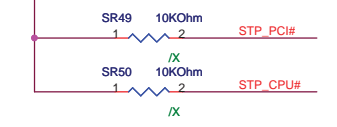
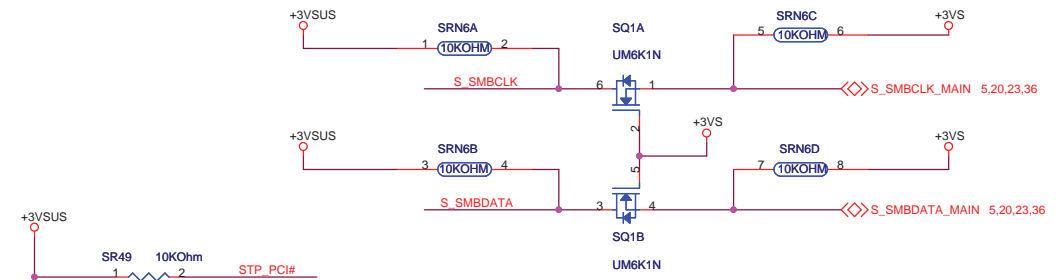


Title : ICH7M-2
Engineer: Endy_Wu

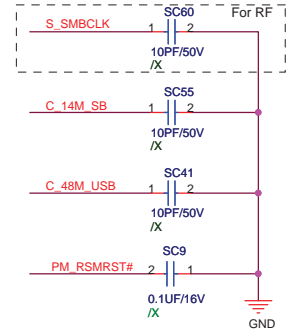
Size	Project Name	Rev
A3	Standard Circuit	0.1B

Date: Thursday, March 19, 2009 Sheet 16 of 48

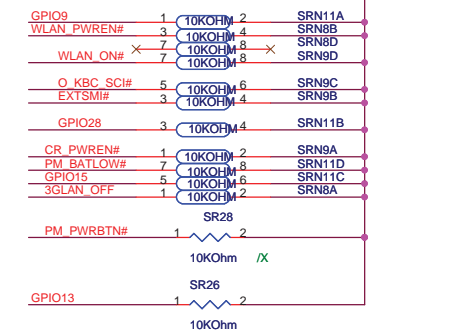
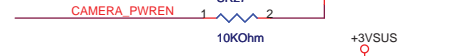
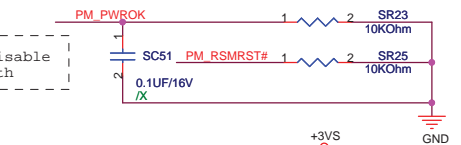




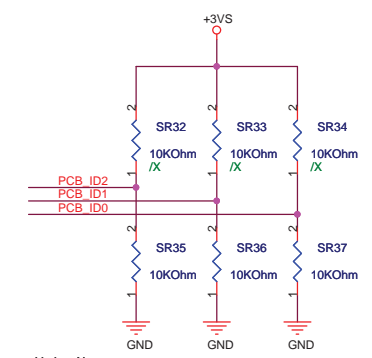
SUI1C		SMB		SYS GPIO	
4	S_SMBCLK	C22	SMBCLK	GPIO21/SATA0GP	AF19
4	S_SMBDATA	B22	SMBDATA	GPIO19/SATA1GP	AH18
		A26	LINKALERT#	GPIO36/SATA2GP	AH19
		B23	SMB_LINK0	GPIO37/SATA3GP	AE19
		A25	SMB_LINK1		
		A28	RING#		
		A19	S_SPKR		
4.5	SYS_RESET#	A27	SUS_STAT#		
		A22	SUS_RST#		
9	PM_BMBUSY#	AB18	GPIO0/BM_BUSY#		
		B23	SMB_ALERT#/GPIO11		
4	STP_PCI#	AC20	GPIO18/STPPCI#		
4	STP_CPU#	AE21	GPIO20/STPCPU#		
		A21	GPIO26		
37	CR_PWREN#	B21	GPIO27		
		E23	GPIO28		
		AG18	GPIO28		
		AC19	GPIO32/CLKRUN#		
		U2	GPIO33/AZ_DOCK_EN#		
		U2	GPIO34/AZ_DOCK_RST#		
27	PCIE_WAKE#	F20	WAKE#		
32	F_SERIRQ	AH21	SERIRQ		
		AE20	THRM#		
		AD22	VRMPWRGD		
		AC24	GPIO6		
		AC18	GPIO7		
		E21	GPIO8		



C_14M_SB	4	C_48M_USB	4	TP_OFF_LED	32,34
PM_SUSB#	25,32	PM_SUSC#	32	3GLAN_OFF	24
PM_PWRVOK	9,32	PM_DPRSLPVR	9,41	PM_BMBUSY#	9
PM_BATLOW#	32	PM_PWRBTN#	32	STP_PCI#	4
PM_PWRTRST#	9,16	SPLTRST#	9,16	STP_CPU#	4
PM_RSMRST#	32	O_KBC_SCI#	32	CR_PWREN#	37
O_KBC_SCI#	32	WLAN_PWREN#	25	PCIE_WAKE#	27
WLAN_PWREN#	25	CAMERA_PWREN	29	F_SERIRQ	32
CAMERA_PWREN	29	S_SMBCLK	4	VRM_PWRGD	32,41
S_SMBCLK	4	S_SMBDATA	4	WLAN_LED	37
S_SMBDATA	4	S_SMBCLK_MAIN	5,20,23,36	EXTSMI#	32
S_SMBCLK_MAIN	5,20,23,36	S_SMBDATA_MAIN	5,20,23,36	SYS_RESET#	4,5
S_SMBDATA_MAIN	5,20,23,36				



PCB_ID[2:0]	PCB Version
0 0 0	R1.0
0 0 1	R1.1
0 1 0	R1.2
0 1 1	R1.3
Others	Reserved

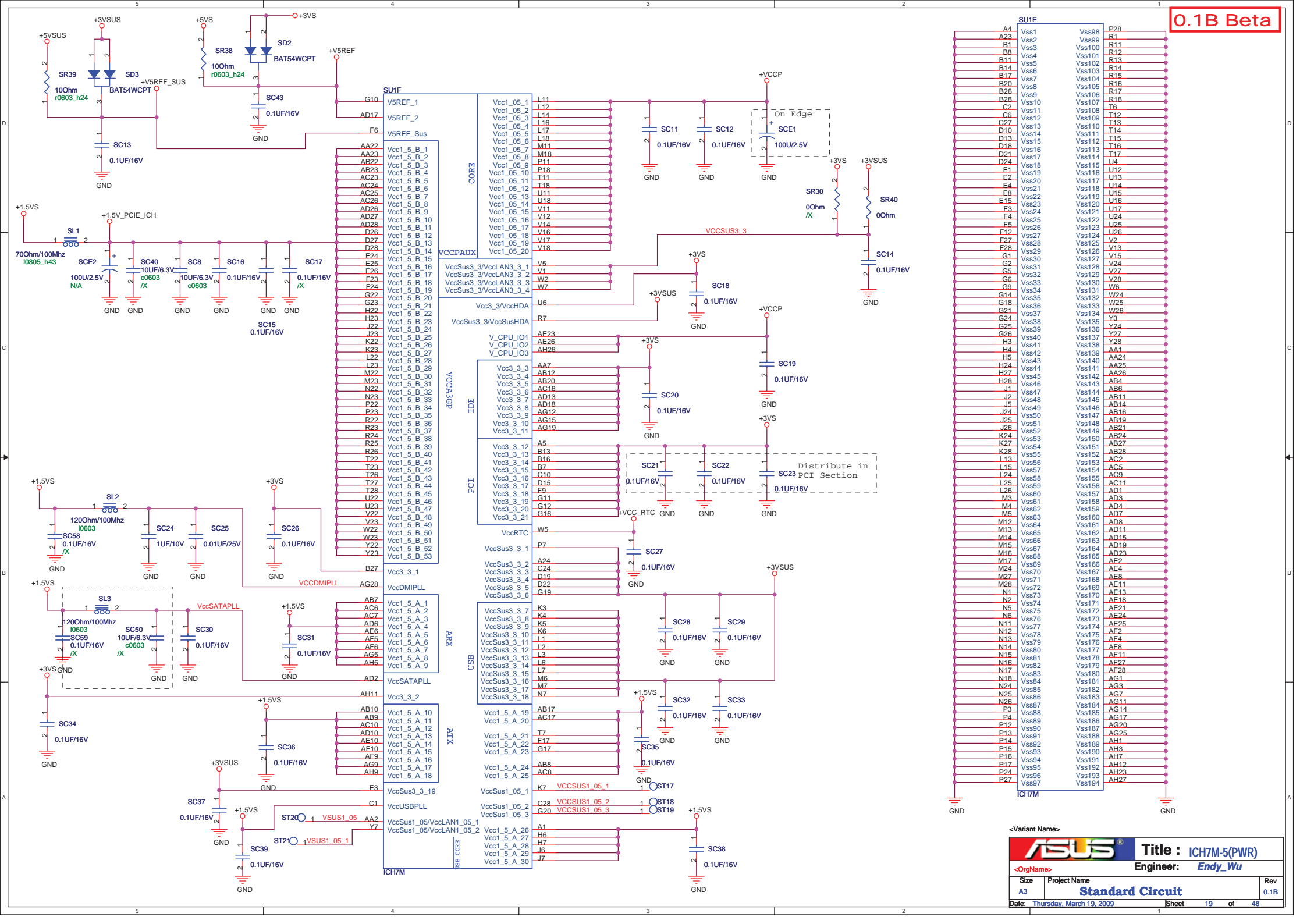


<Variant Name>

ASUS Title: ICH7M-4(GPIO) Engineer: Endy_Wu


Size: A3 Project Name: Standard Circuit Rev: 0.1B

Date: Thursday, March 19, 2009 Sheet: 18 of 48



SUIE		
A4	Vss1	P28
A23	Vss2	R1
B1	Vss3	Vss99
B8	Vss4	Vss100
B11	Vss5	Vss101
B14	Vss6	Vss102
B17	Vss7	Vss103
B20	Vss8	Vss104
B26	Vss9	Vss105
B28	Vss10	Vss106
C2	Vss11	Vss107
C6	Vss12	Vss108
C27	Vss13	Vss109
D10	Vss14	Vss110
D13	Vss15	Vss111
D18	Vss16	Vss112
D21	Vss17	Vss113
D24	Vss18	Vss114
E1	Vss19	Vss115
E2	Vss20	Vss116
E4	Vss21	Vss117
E15	Vss22	Vss118
F3	Vss23	Vss119
F4	Vss24	Vss120
F5	Vss25	Vss121
F12	Vss26	Vss122
F22	Vss27	Vss123
F28	Vss28	Vss124
G1	Vss29	Vss125
G2	Vss30	Vss126
G5	Vss31	Vss127
G6	Vss32	Vss128
G9	Vss33	Vss129
G14	Vss34	Vss130
G18	Vss35	Vss131
G21	Vss36	Vss132
G24	Vss37	Vss133
G25	Vss38	Vss134
G26	Vss39	Vss135
H3	Vss40	Vss136
H4	Vss41	Vss137
H5	Vss42	Vss138
H24	Vss43	Vss139
H27	Vss44	Vss140
H28	Vss45	Vss141
J1	Vss46	Vss142
J5	Vss47	Vss143
J24	Vss48	Vss144
J25	Vss49	Vss145
J26	Vss50	Vss146
K24	Vss51	Vss147
K27	Vss52	Vss148
K28	Vss53	Vss149
L13	Vss54	Vss150
L15	Vss55	Vss151
L24	Vss56	Vss152
L25	Vss57	Vss153
L26	Vss58	Vss154
M3	Vss59	Vss155
M4	Vss60	Vss156
M5	Vss61	Vss157
M12	Vss62	Vss158
M13	Vss63	Vss159
M14	Vss64	Vss160
M16	Vss65	Vss161
M17	Vss66	Vss162
M24	Vss67	Vss163
M27	Vss68	Vss164
M28	Vss69	Vss165
N1	Vss70	Vss166
N2	Vss71	Vss167
N5	Vss72	Vss168
N6	Vss73	Vss169
N11	Vss74	Vss170
N12	Vss75	Vss171
N13	Vss76	Vss172
N14	Vss77	Vss173
N15	Vss78	Vss174
N16	Vss79	Vss175
N17	Vss80	Vss176
N18	Vss81	Vss177
N24	Vss82	Vss178
N25	Vss83	Vss179
N26	Vss84	Vss180
P3	Vss85	Vss181
P4	Vss86	Vss182
P12	Vss87	Vss183
P13	Vss88	Vss184
P14	Vss89	Vss185
P16	Vss90	Vss186
P17	Vss91	Vss187
P24	Vss92	Vss188
P27	Vss93	Vss189
	Vss94	Vss190
	Vss95	Vss191
	Vss96	Vss192
	Vss97	Vss193
	Vss98	Vss194

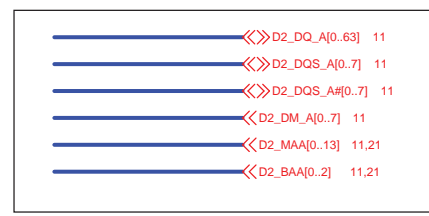
<Variant Name>



Title : ICH7M-5(PWR)
Engineer: Endy_Wu

Size	Project Name	Rev
A3	Standard Circuit	0.1B

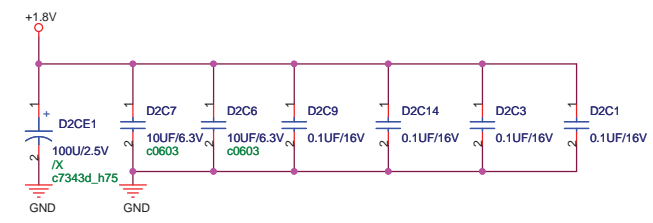
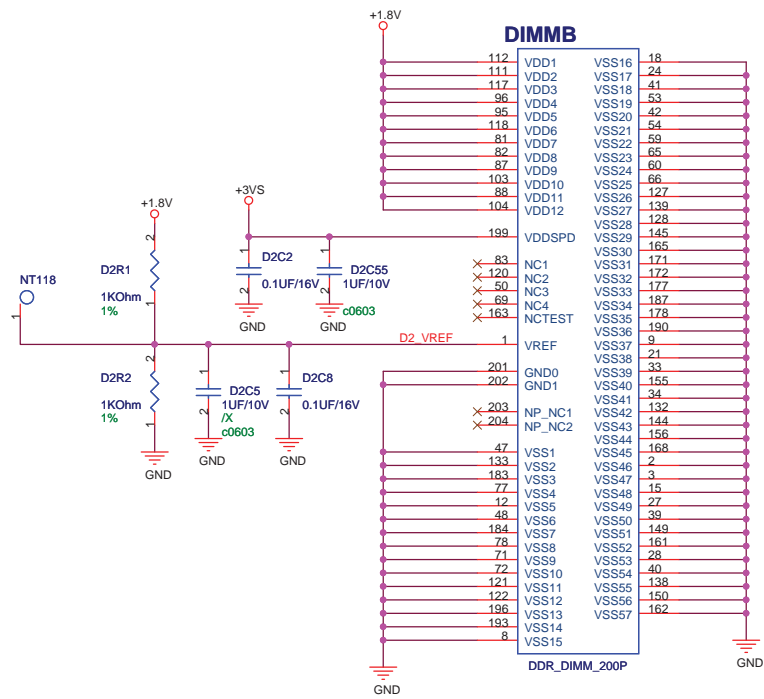
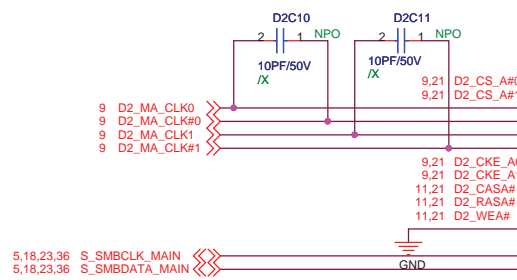
Date: Thursday, March 19, 2009 Sheet 19 of 48



DIMMA

D2_MAA0	102	A0	DQ0	5	D2_DQ_A0
D2_MAA1	101	A1	DQ1	7	D2_DQ_A1
D2_MAA2	100	A2	DQ2	17	D2_DQ_A2
D2_MAA3	99	A3	DQ3	19	D2_DQ_A3
D2_MAA4	98	A4	DQ4	4	D2_DQ_A4
D2_MAA5	97	A5	DQ5	6	D2_DQ_A5
D2_MAA6	94	A6	DQ6	14	D2_DQ_A6
D2_MAA7	92	A7	DQ7	16	D2_DQ_A7
D2_MAA8	93	A8	DQ8	23	D2_DQ_A8
D2_MAA9	91	A8	DQ8	25	D2_DQ_A9
D2_MAA10	105	A9	DQ9	35	D2_DQ_A10
D2_MAA11	90	A10/AP	DQ10	37	D2_DQ_A11
D2_MAA12	89	A12	DQ12	20	D2_DQ_A12
D2_MAA13	116	A13	DQ13	22	D2_DQ_A13
	86	A14	DQ14	38	D2_DQ_A14
	84	A15	DQ15	38	D2_DQ_A15
D2_BAA2	85	A16_BA2	DQ16	43	D2_DQ_A16
			DQ17	45	D2_DQ_A17
D2_BAA0	107	BA0	DQ18	55	D2_DQ_A18
D2_BAA1	106	BA1	DQ19	57	D2_DQ_A19
	110	S0#	DQ20	44	D2_DQ_A20
	36	S1#	DQ21	46	D2_DQ_A21
	166	CK1#	DQ22	58	D2_DQ_A22
	79	CKE0	DQ23	61	D2_DQ_A23
9,21 D2_CKE_A0	80	CKE1	DQ24	61	D2_DQ_A24
9,21 D2_CKE_A1	115	CAS#	DQ25	63	D2_DQ_A25
11,21 D2_CASA#	113	RAS#	DQ26	73	D2_DQ_A26
11,21 D2_RASA#	108	WE#	DQ27	75	D2_DQ_A27
11,21 D2_WEA#	109	SA0	DQ28	64	D2_DQ_A28
	198	SA1	DQ29	74	D2_DQ_A29
	200	SCL	DQ30	76	D2_DQ_A30
5,18,23,36 S_SMBCLK_MAIN	195	SDA	DQ31	76	D2_DQ_A31
5,18,23,36 S_SMBDATA_MAIN			DQ32	123	D2_DQ_A32
			DQ33	125	D2_DQ_A33
			DQ34	135	D2_DQ_A34
			DQ35	137	D2_DQ_A35
			DQ36	124	D2_DQ_A36
9,21 D2_ODT_A0	114	ODT0	DQ37	126	D2_DQ_A37
9,21 D2_ODT_A1	119	ODT1	DQ38	134	D2_DQ_A38
			DQ39	136	D2_DQ_A39
D2_DM_A0	10	DM0	DQ40	141	D2_DQ_A40
D2_DM_A1	26	DM1	DQ41	143	D2_DQ_A41
D2_DM_A2	52	DM2	DQ42	151	D2_DQ_A42
D2_DM_A3	67	DM3	DQ43	153	D2_DQ_A43
D2_DM_A4	130	DM4	DQ44	140	D2_DQ_A44
D2_DM_A5	147	DM5	DQ45	142	D2_DQ_A45
D2_DM_A6	170	DM6	DQ46	152	D2_DQ_A46
D2_DM_A7	185	DM7	DQ47	154	D2_DQ_A47
			DQ48	157	D2_DQ_A48
			DQ49	159	D2_DQ_A49
D2_DQS_A0	13	DQS0	DQ50	173	D2_DQ_A50
D2_DQS_A1	31	DQS1	DQ51	175	D2_DQ_A51
D2_DQS_A2	51	DQS2	DQ52	158	D2_DQ_A52
D2_DQS_A3	70	DQS3	DQ53	160	D2_DQ_A53
D2_DQS_A4	131	DQS4	DQ54	174	D2_DQ_A54
D2_DQS_A5	148	DQS5	DQ55	176	D2_DQ_A55
D2_DQS_A6	169	DQS6	DQ56	179	D2_DQ_A56
D2_DQS_A7	188	DQS7	DQ57	181	D2_DQ_A57
D2_DQS_A#0	11	DQS#0	DQ58	189	D2_DQ_A58
D2_DQS_A#1	29	DQS#1	DQ59	191	D2_DQ_A59
D2_DQS_A#2	49	DQS#2	DQ60	180	D2_DQ_A60
D2_DQS_A#3	68	DQS#3	DQ61	182	D2_DQ_A61
D2_DQS_A#4	129	DQS#4	DQ62	192	D2_DQ_A62
D2_DQS_A#5	146	DQS#5	DQ63	194	D2_DQ_A63
D2_DQS_A#6	167	DQS#6			
D2_DQS_A#7	186	DQS#7			

DDR_DIMM_200P

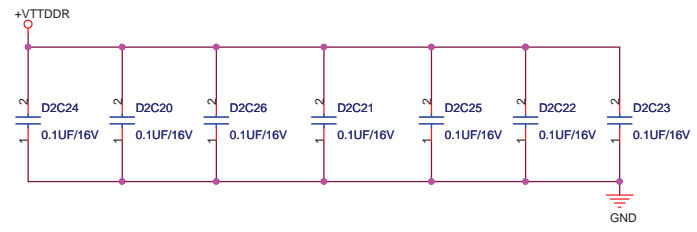
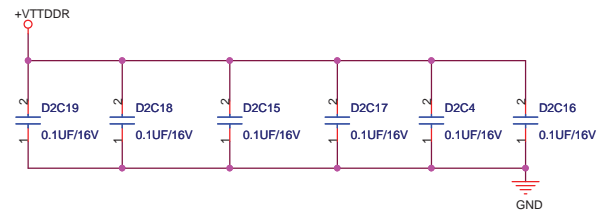
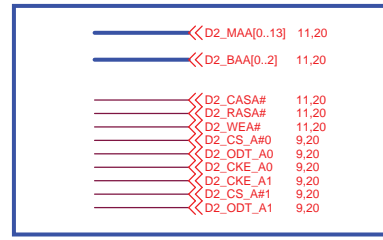
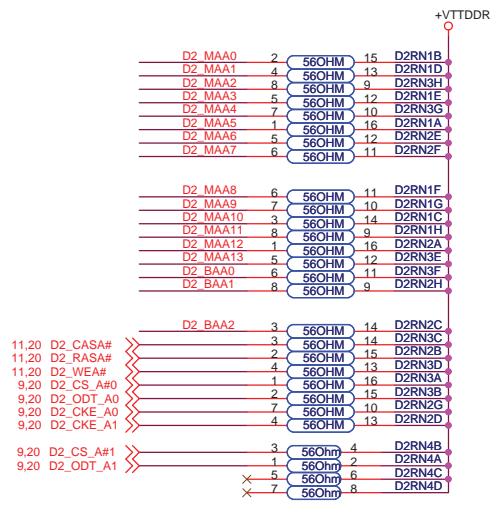


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ASUS Title : **DDR2-SO-DIMM**
 ASUSTek Computer INC. Engineer: **Endy_Wu**

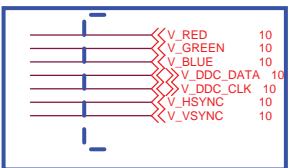
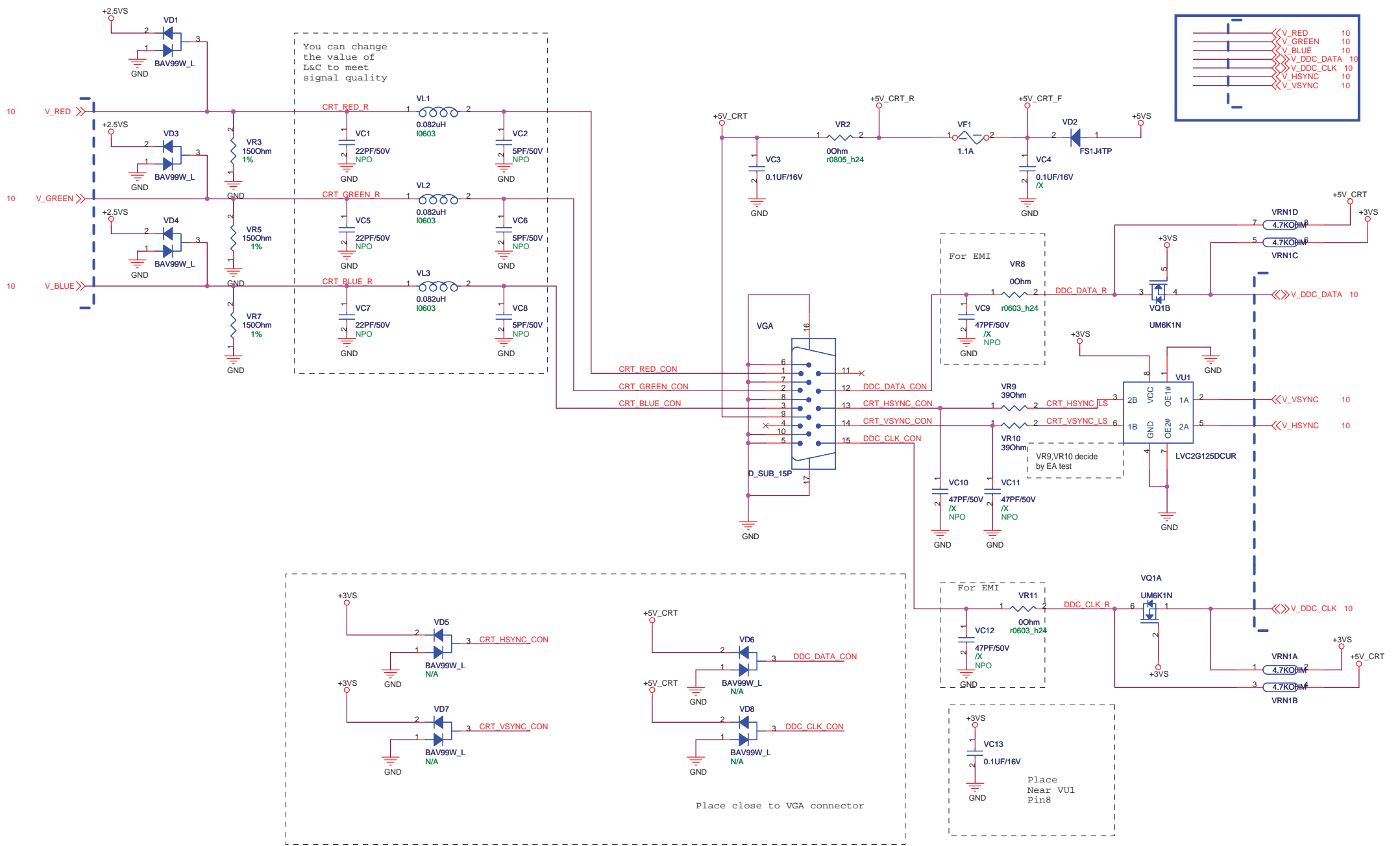
Size	Project Name	Rev
A3	Standard Circuit	0.1B

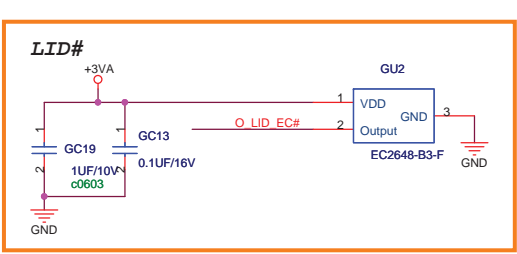
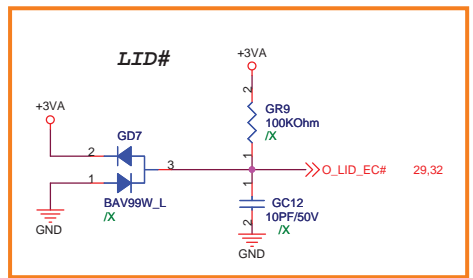
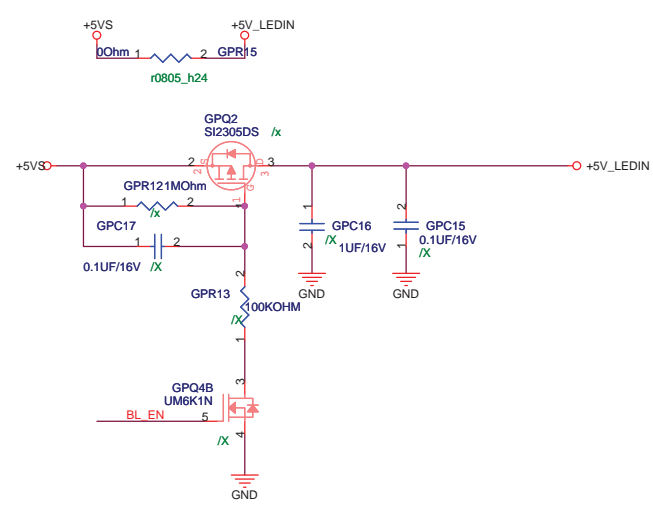
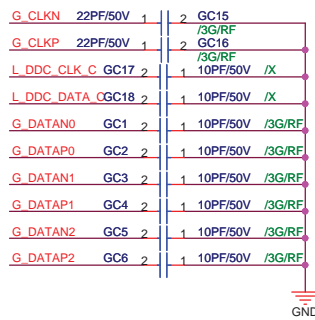
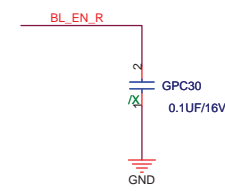
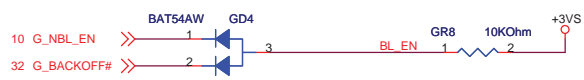
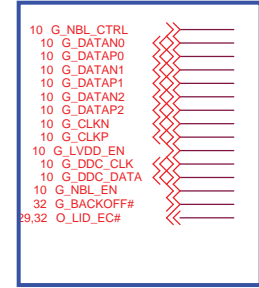
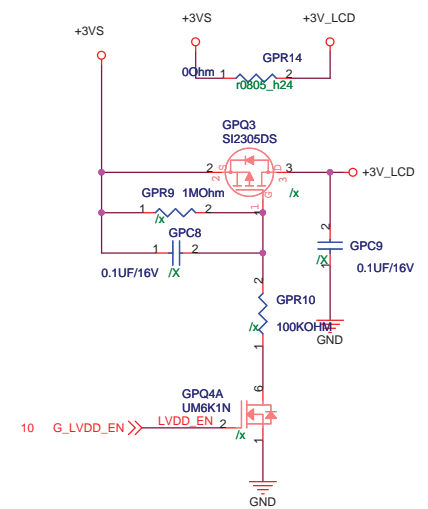
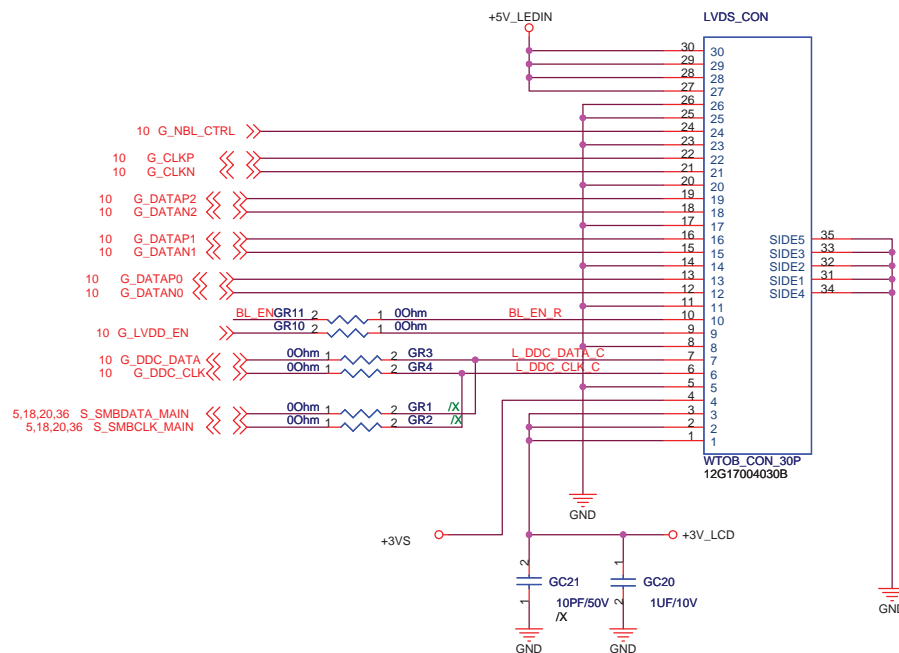
Date: Thursday, March 19, 2009 Sheet 20 of 48



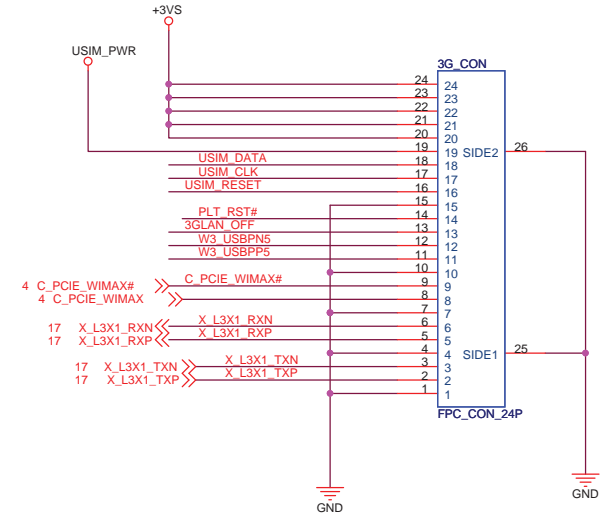
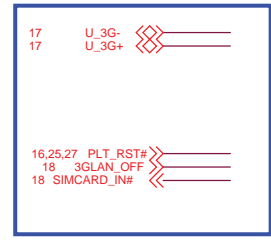
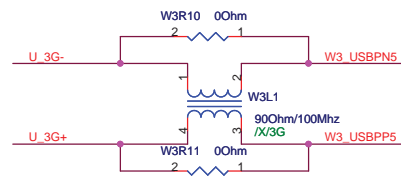
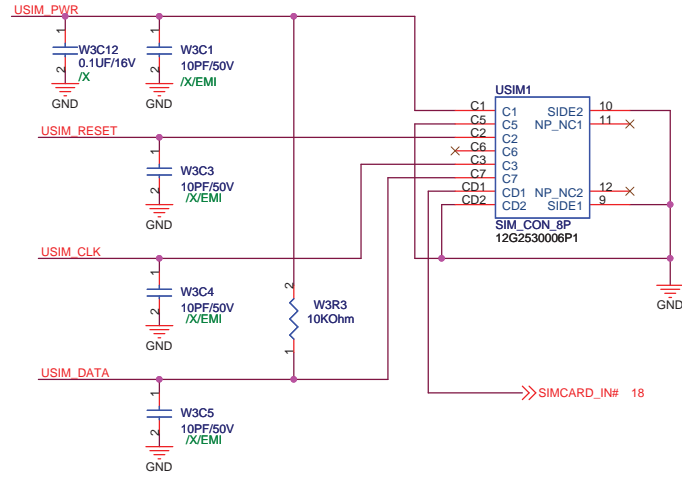
<Variant Name>

		Title : DDR2-Termination
ASUSTek Computer INC.		Engineer: Endy_Wu
Size A3	Project Name Standard Circuit	Rev 0.1B
Date: Thursday, March 19, 2009	Sheet 21	of 48



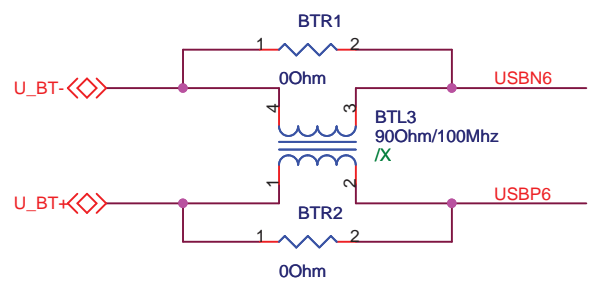


CAP Near SIM Socket

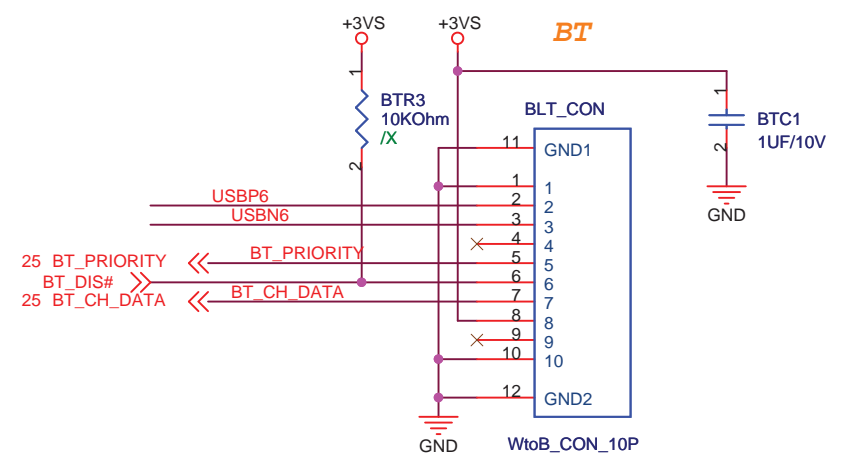


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17

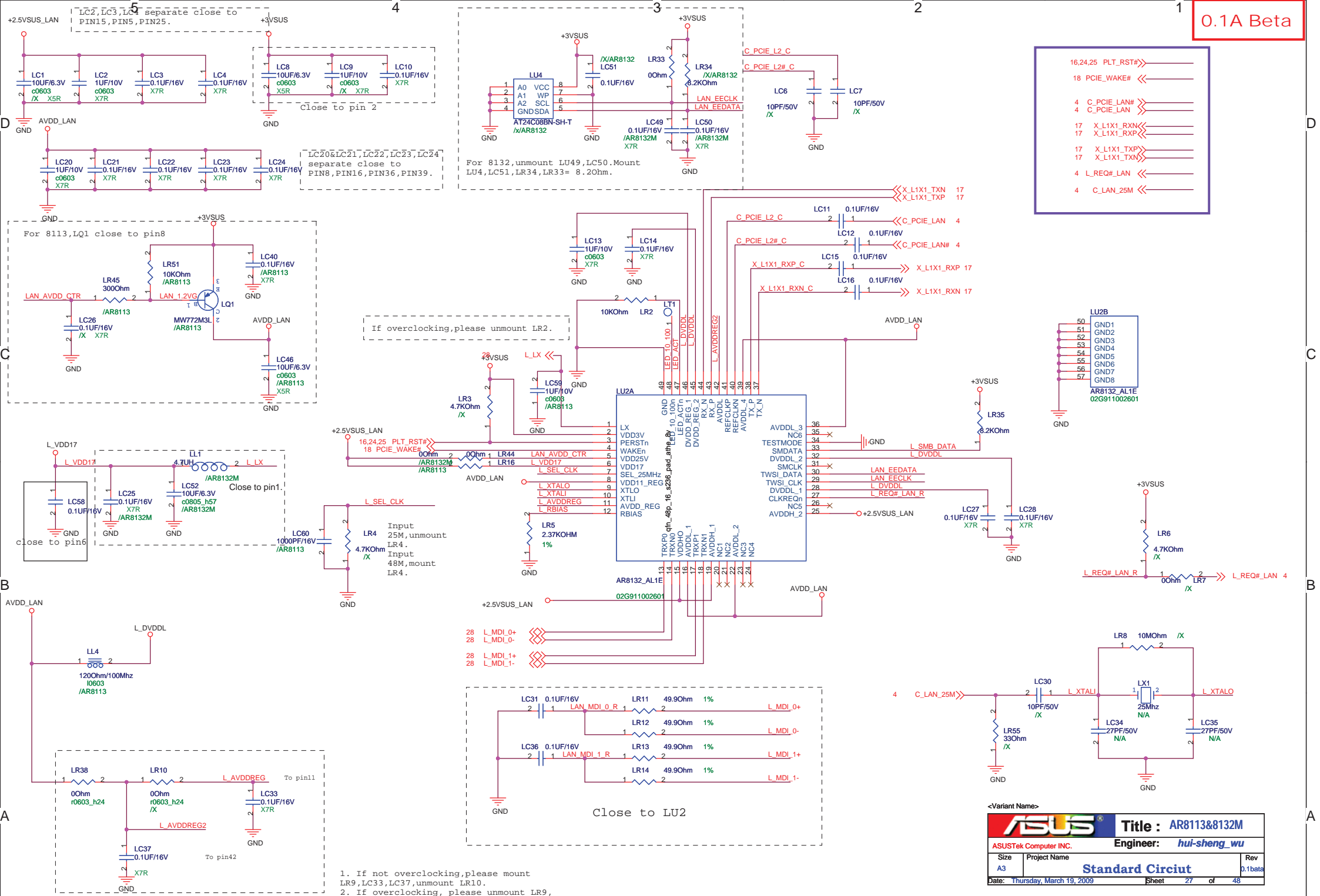


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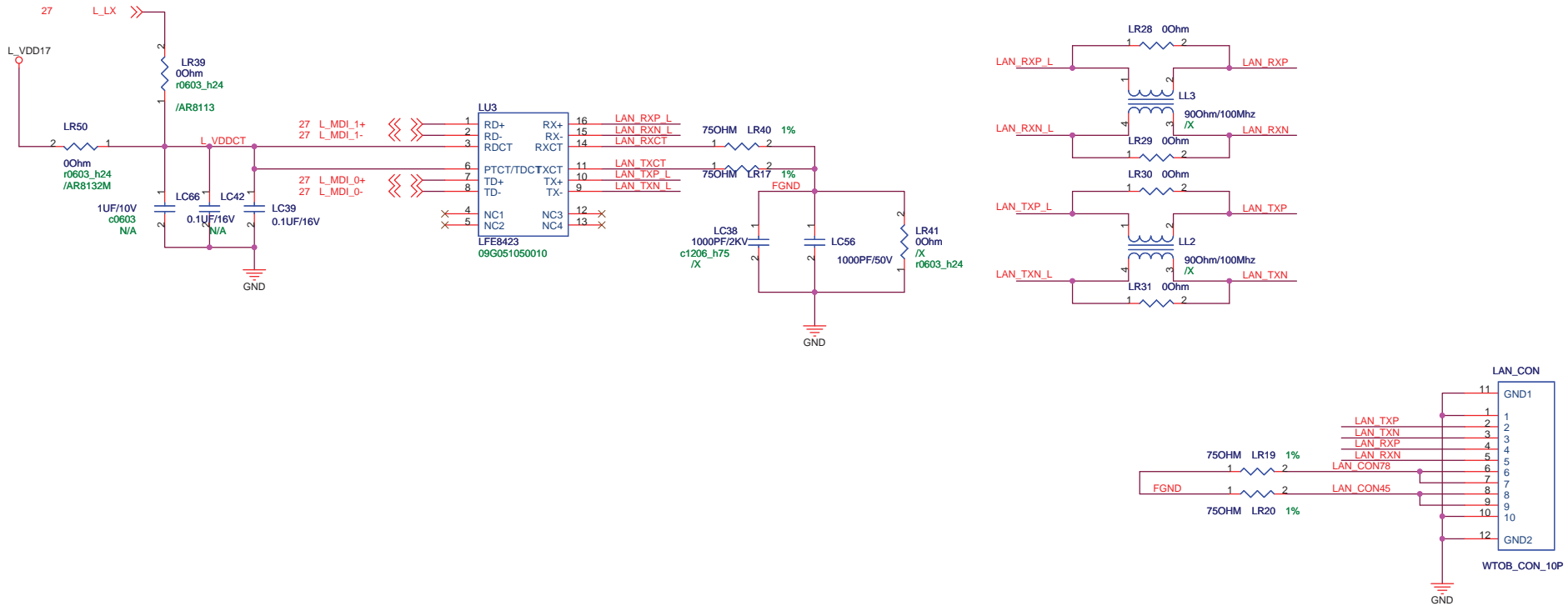
<Variant Name>

		Title : BLUETOOTH	
ASUSTek Computer INC.		Engineer: JOE1_ZHOU	
Size A4	Project Name Standard Circiut		Rev 0.1A
Date: Thursday, March 19, 2009		Sheet	26 of 48



1. If not overclocking, please mount LR9, LC33, LC37, unmount LR10.
2. If overclocking, please unmount LR9, mount LR10, LC33, LC37.

ASUS		Title : AR8113&8132M	
ASUSTek Computer INC.		Engineer: hui-sheng wu	
Size A3	Project Name Standard Circuit	Rev 0.1beta	
Date: Thursday, March 19, 2009	Sheet 27	of 48	



<Variant Name>

ASUS		Title : RJ45
ASUSTek Computer INC.		Engineer: <i>Hui-sheng_wu</i>
Size A3	Project Name Standard Circuit	Rev 0.1A
Date: Thursday, March 19, 2009	Sheet 28 of 48	

17 U_CAM+ <<>
 17 U_CAM- <<>
 18 CAMERA_PWREN >>>

17 U_USB4+ <<>
 17 U_USB4- <<>
 17 U_USB5+ <<>
 17 U_USB5- <<>
 17 U_USBOC#45 <<>

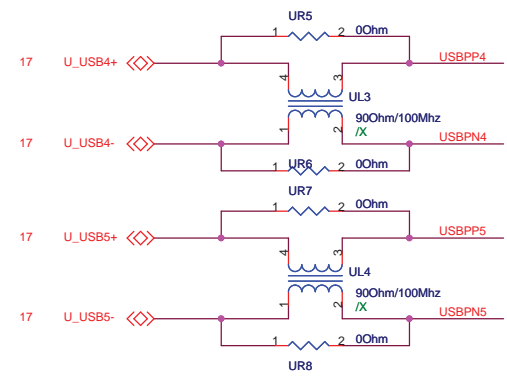
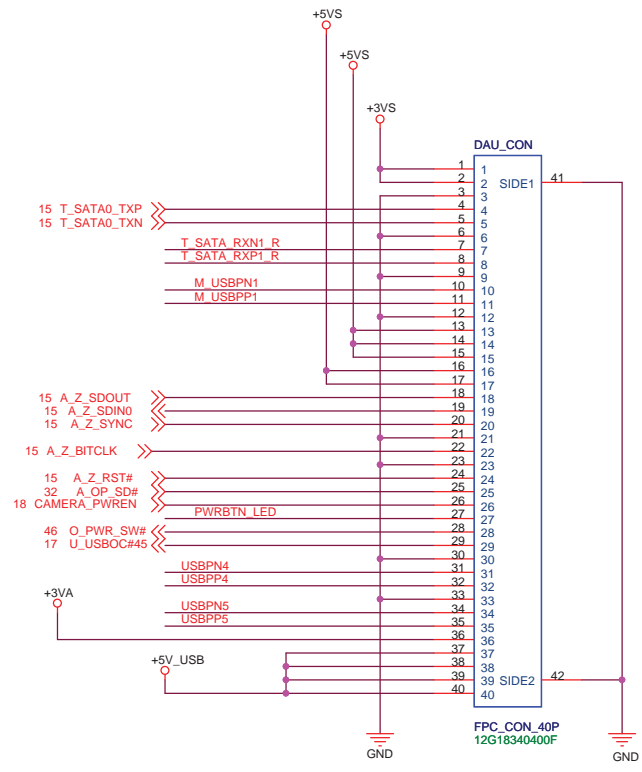
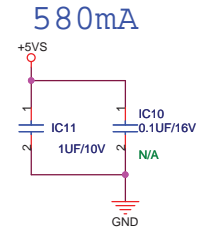
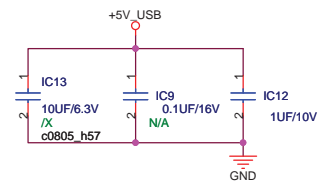
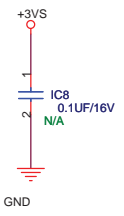
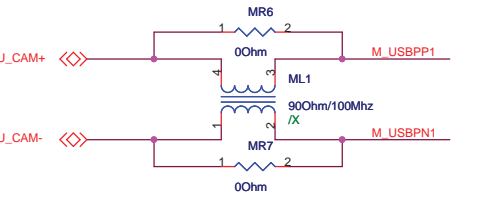
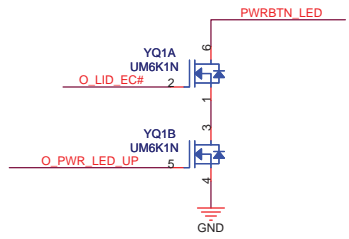
15 A_Z_SDOOUT >>>
 15 A_Z_BITCLK >>>
 15 A_Z_SDIN0 >>>
 15 A_Z_SYNC >>>
 15 A_Z_RST# >>>

32 A_OP_SD# >>>

46 O_PWR_SW# >>>

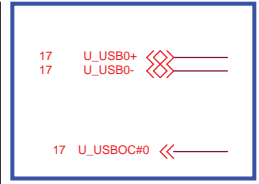
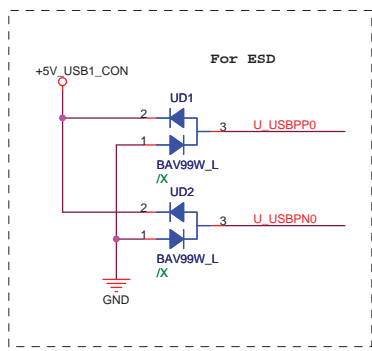
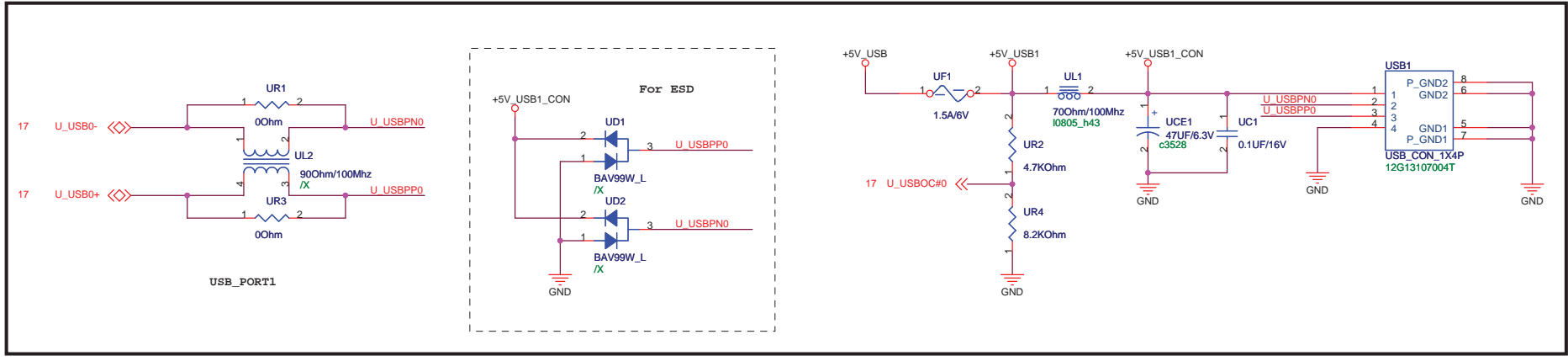
32,37 O_PWR_LED_UP <<<

23,32 O_LID_EC# >>>




<Variant Name>

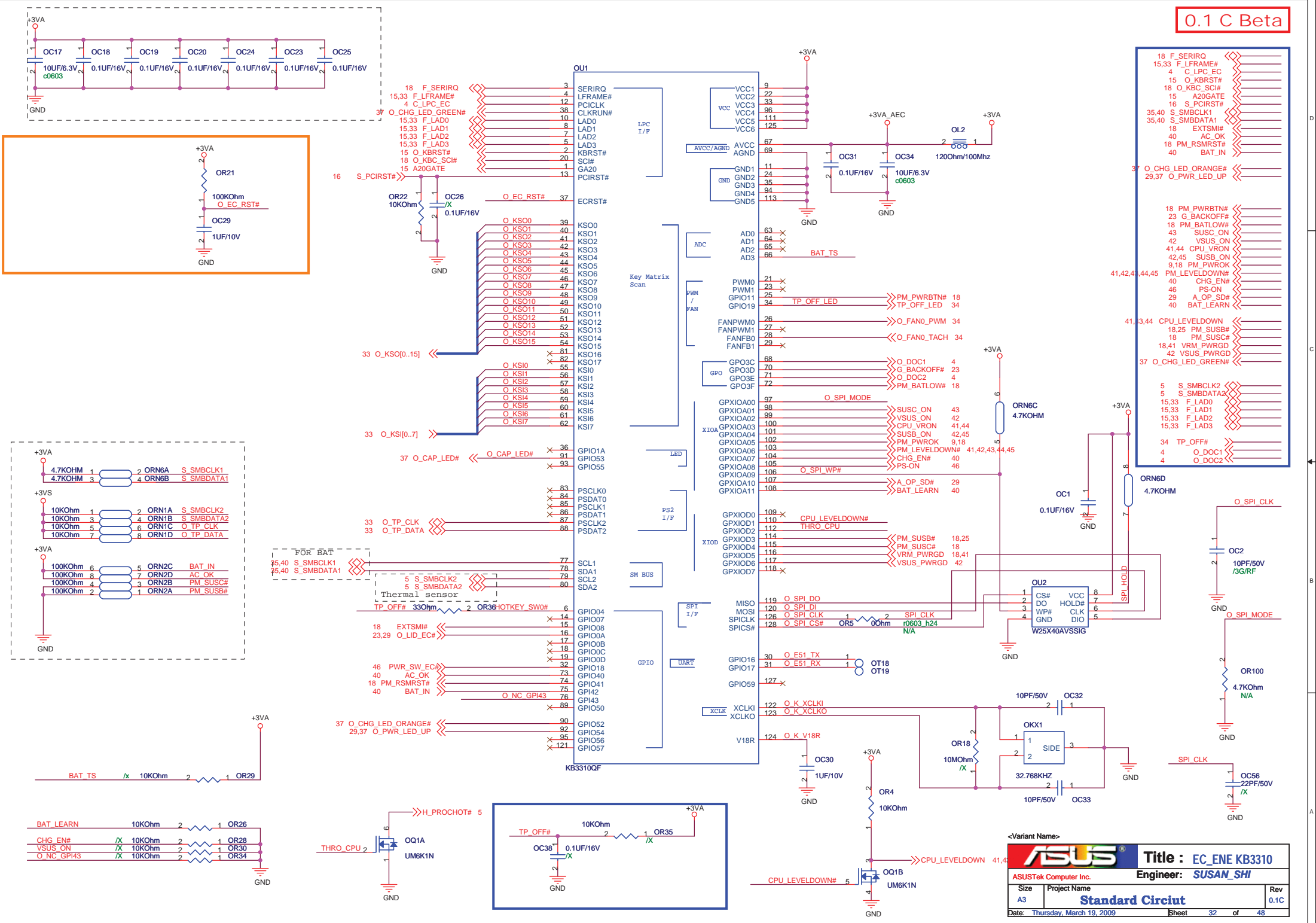
		Title : SATA HDD	
ASUSTek Computer INC.		Engineer: KingCa_Jin	
Size	Project Name	Rev	
A3	1000HN	1.0	
Date: Thursday, March 19, 2009	Sheet	29	of 48





<Variant Name>

		Title : Camera CONN	
ASUSTEK COMPUTER INC		Engineer: KEN_JIN	
Size	Project Name		Rev
A3	Standard Circuit		0.1A
Date: Thursday, March 19, 2009		Sheet	31 of 48



18	F_SERIRQ	3
15,33	F_LFRAME#	4
4	C_LPC_EC	12
15	O_KBRST#	38
18	O_KBC_SCH#	10
15	A20GATE	7
16	S_PCIRST#	7
35,40	S_SMBCLK1	5
35,40	S_SMBDATA1	2
18	EXTSMI#	20
40	AC_OK	1
18	PM_RSMRST#	2
40	BAT_IN	13
37	O_CHG_LED_ORANGE#	37
29,37	O_PWR_LED_UP	37
18	PM_PWRBTN#	39
23	G_BACKOFF#	41
18	PM_BATLOW#	42
43	SUSC_ON	43
42	VSUS_ON	43
41,44	CPU_VRON	41,44
42,45	SUSB_ON	42,45
9,18	PM_PWROK	9,18
18,25	PM_LEVELDOWN#	18,25
40	CHG_EN#	40
46	PS_ON	46
29	A_OP_SD#	29
40	BAT_LEARN	40
41,34	CPU_LEVELDOWN	41,34
18,25	PM_SUSB#	18,25
18	PM_SUSC#	18
18,41	VRM_PWRGD	18,41
42	VSUS_PWRGD	42
37	O_CHG_LED_GREEN#	37
5	S_SMBCLK2	5
5	S_SMBDATA2	5
15,33	F_LAD0	7
15,33	F_LAD1	7
15,33	F_LAD2	7
15,33	F_LAD3	7
34	TP_OFF#	34
4	O_DOC1	4
4	O_DOC2	4

<Variant Name>

ASUS Title: EC_ENE KB3310

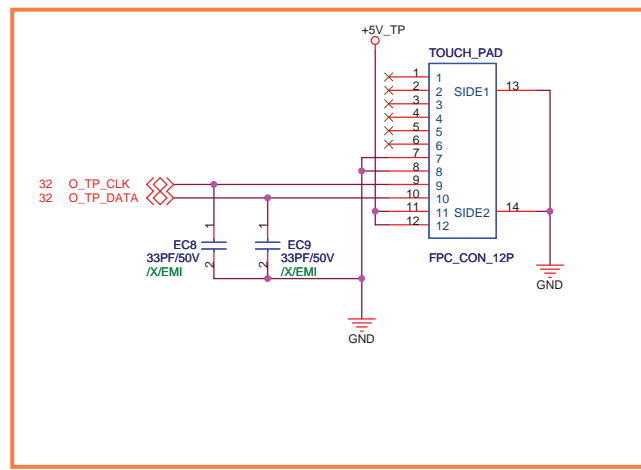
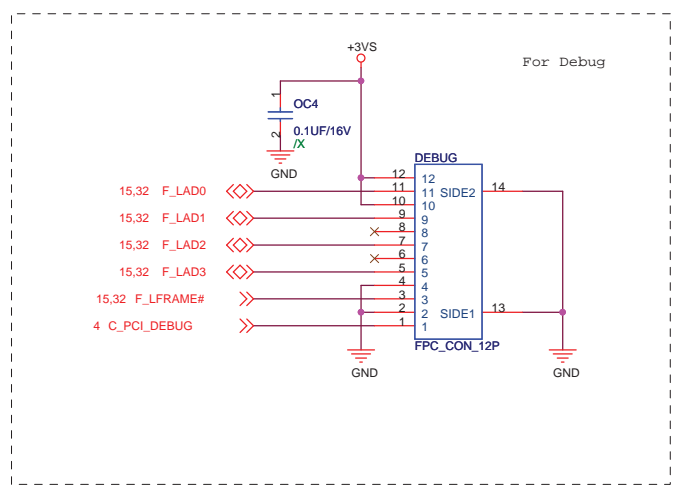
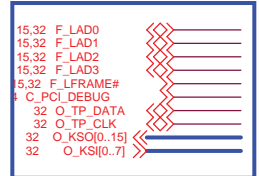
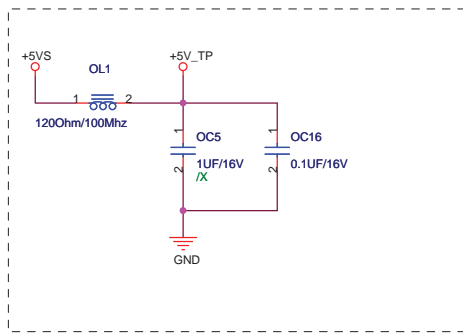
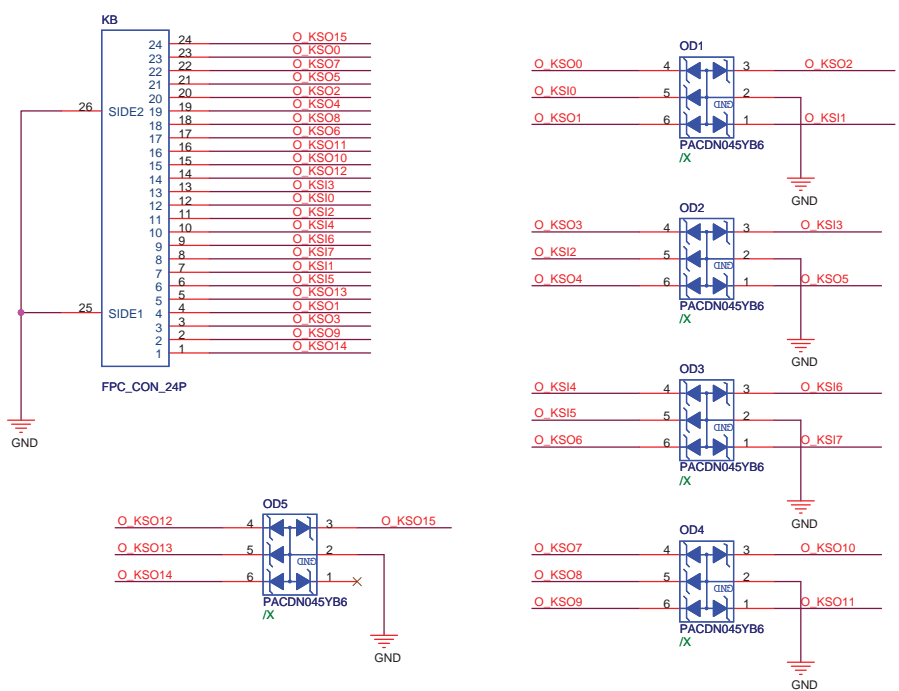
ASUSTek Computer Inc. Engineer: SUSAN_SHI

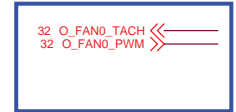
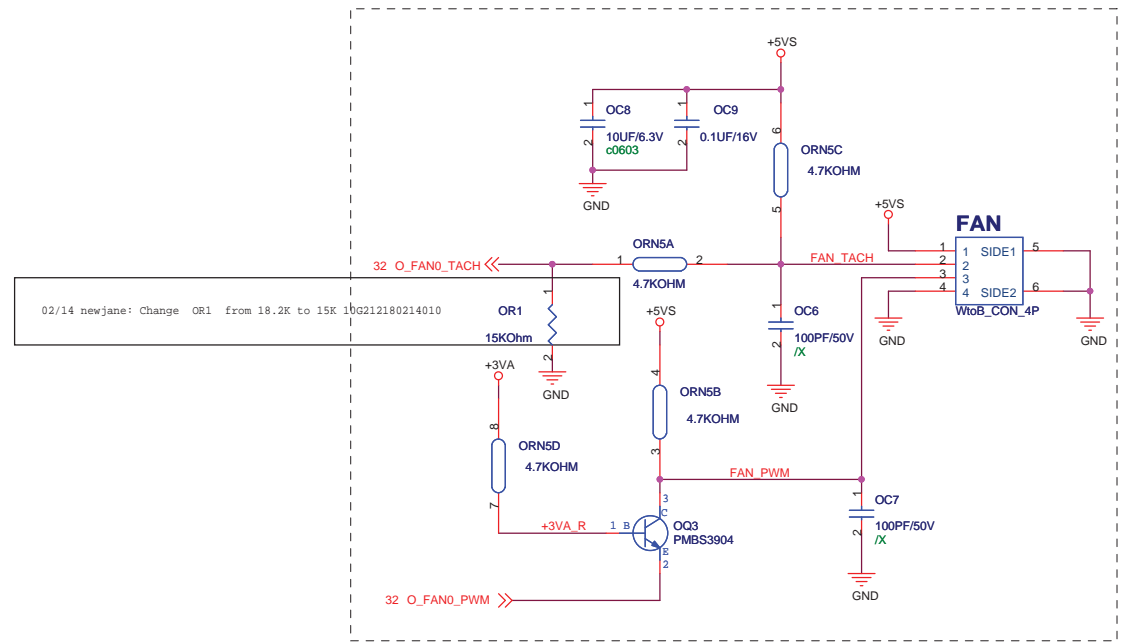
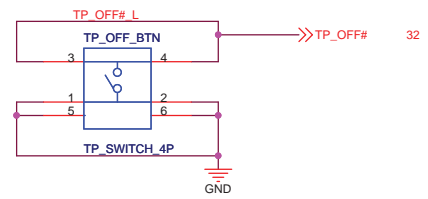
Size	Project Name	Rev
A3	Standard Circuit	0.1C

Date: Thursday, March 19, 2009 Sheet 32 of 48

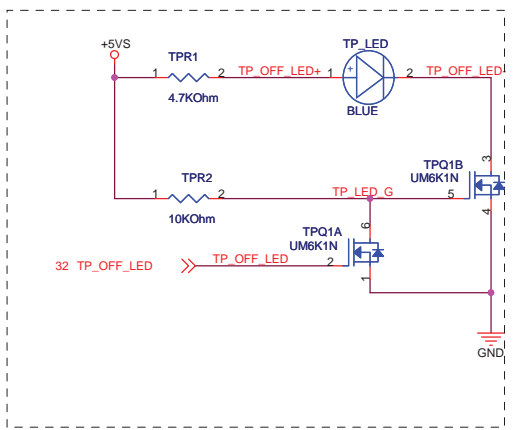
→ O_KSO[0..15] 32
 ← O_KSI[0..7] 32

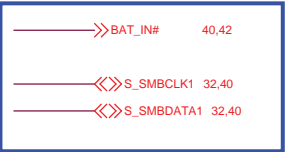
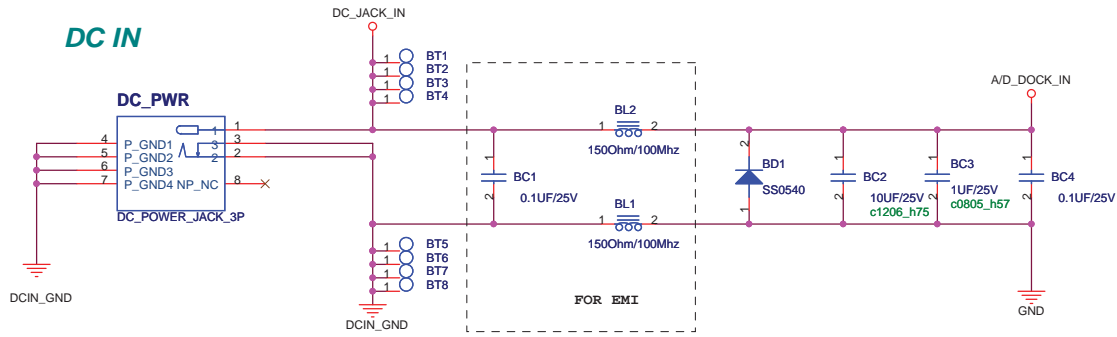
For Keyboard Connector



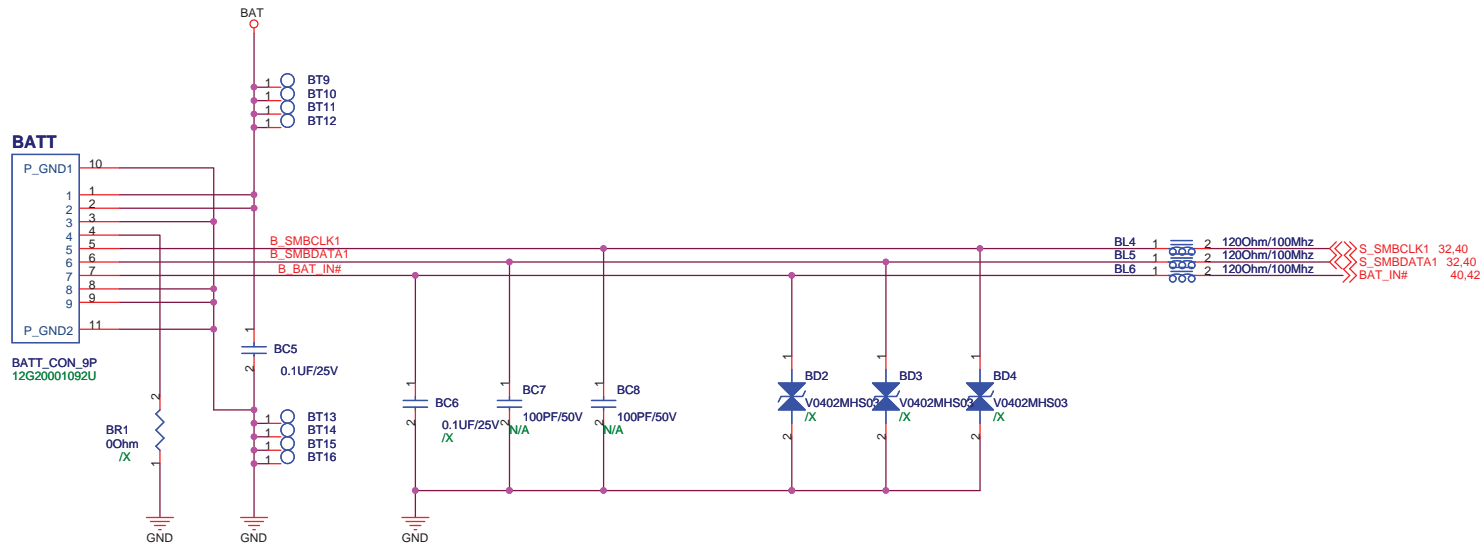


For TP LED



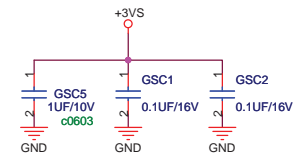
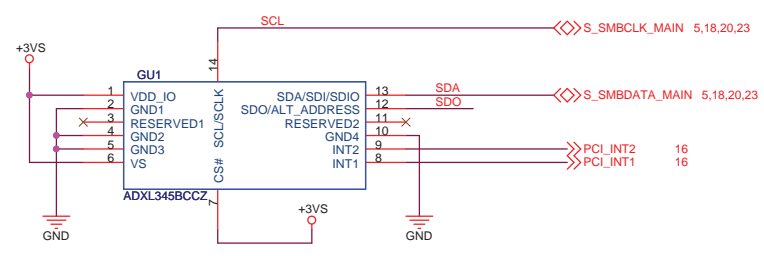
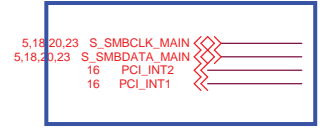


change from DIP to SMD



<Variant Name>

ASUS		Title : PWR Jack
ASUSTEK COMPUTER INC		Engineer: KEN_JIN
Size	Project Name	Rev
A3	Standard Circiut	0.1B
Date: Thursday, March 19, 2009	Sheet 35 of 48	



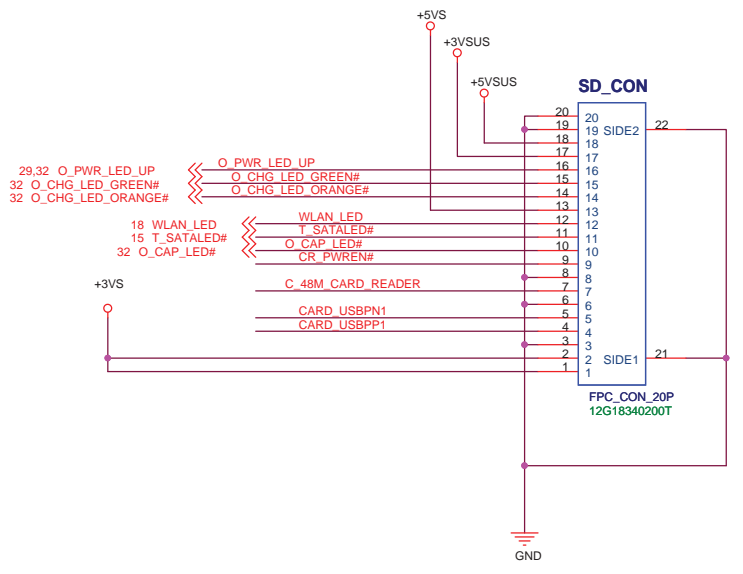
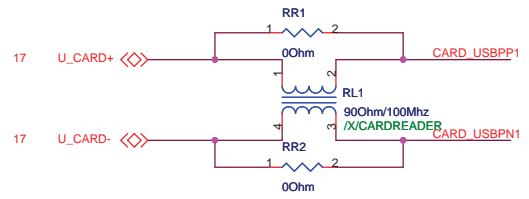
Install GSR6 being slave address "3A" for ADI/Freescale/ST G-sensors

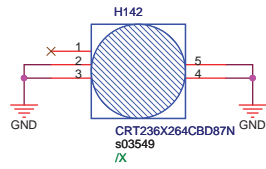
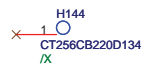
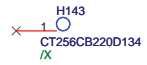
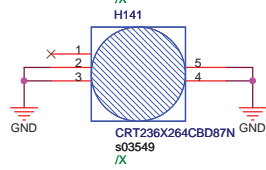
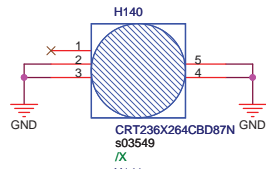
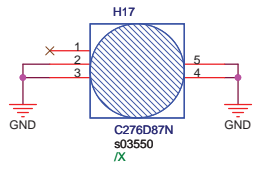
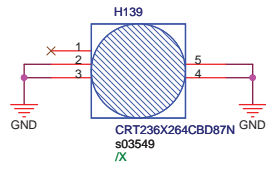
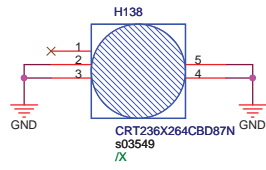
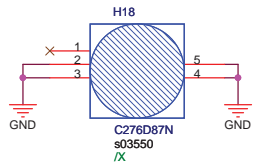


<Variant Name>

		Title : G_sensor	
ASUSTek Computer Inc.		Engineer: SUSAN_SHI	
Size A3	Project Name Standard Circuit	Date Thursday, March 19, 2009	Rev 0.1A
		Sheet 36	of 48

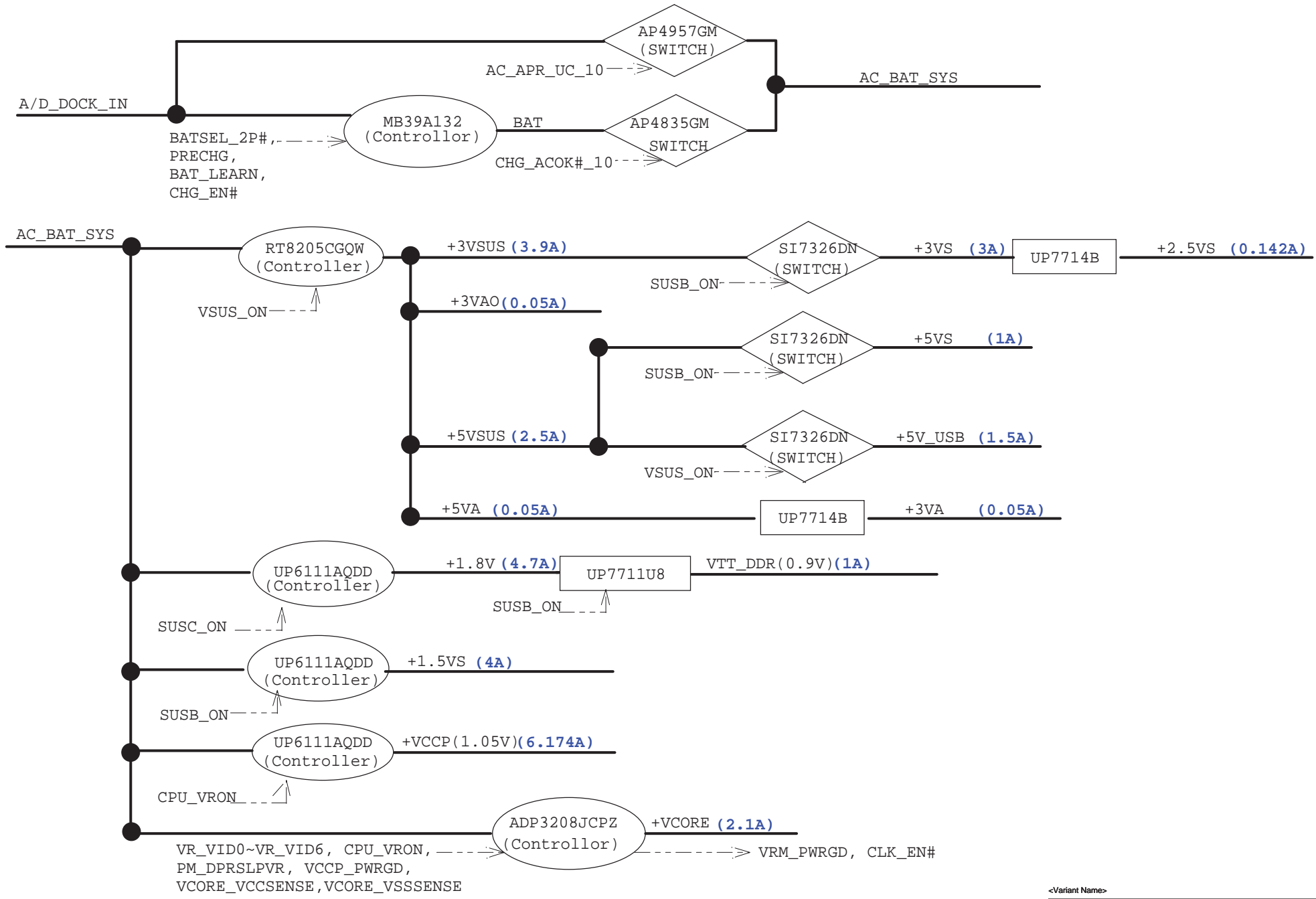
- 4 C_48M_CARD_READER
- 17 U_CARD+
- 17 U_CARD-
- 18 CR_PWREN#

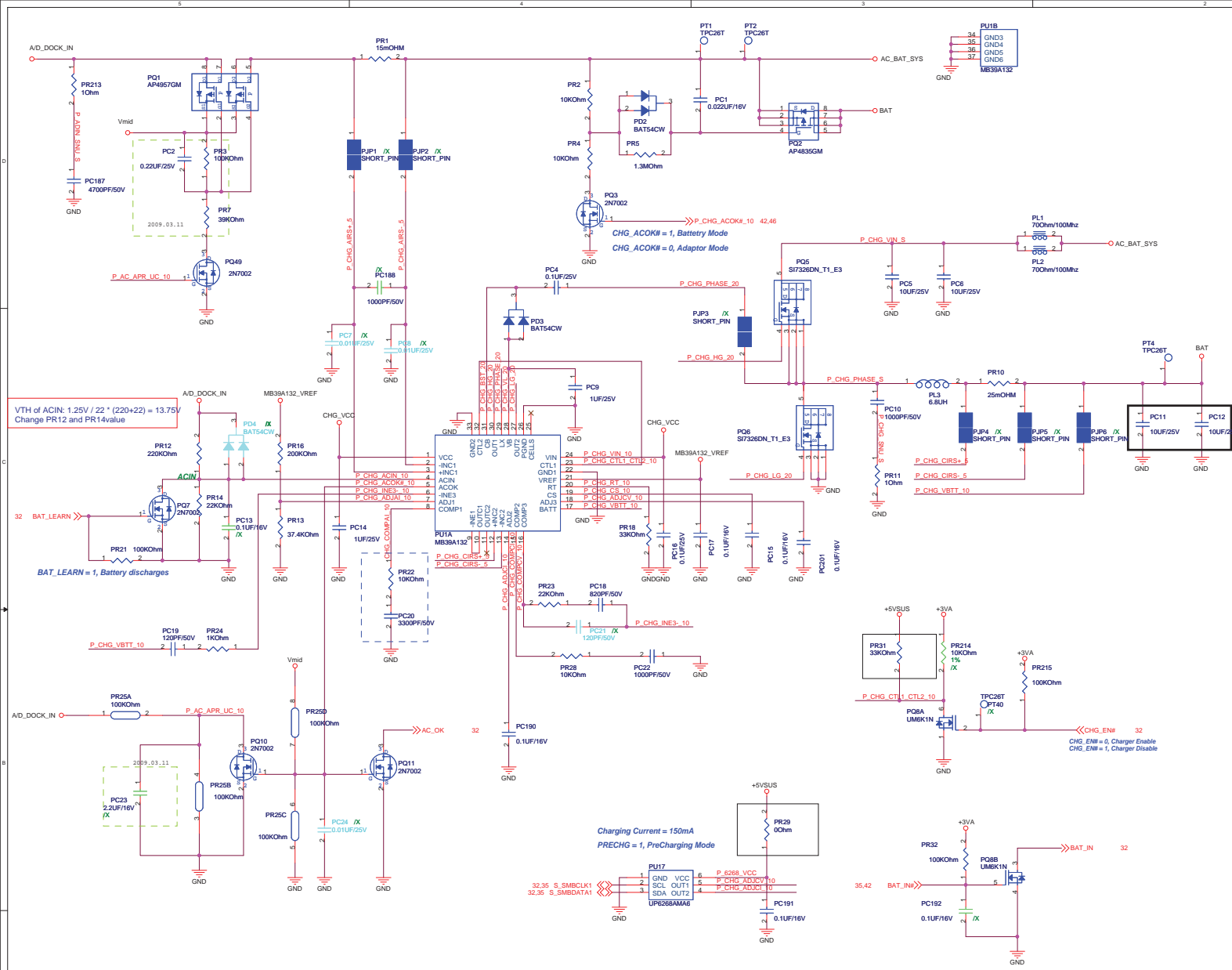




<Variant Name>

		Title : Srew Hole	
ASUSTek Computer INC.		Engineer: Kell_Huang	
Size	Project Name		Rev
A3	1005HN_MN		1.0G
Date: Thursday, March 19, 2009		Sheet	38 of 48





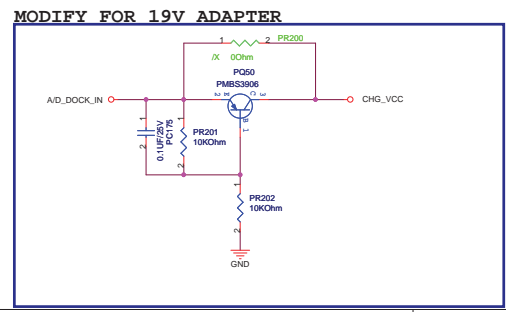
Power stage

- I/P Current:**
 $I_{in} = V_o \cdot I_o / (0.8 \cdot V_{in}) = 1.64A$
- Ripple Current:**
 $I_{rip} = 1.18A$
 $I_{spec} = 2A \odot 1$

pcs
- Inductor Spec:**
 $I_{sat} = 10A$
 $I_{dc} = 5.5A$
 $DCR = 37mohm$
- MOSFET Spec:**
H-side MOSFET: SI7326DN_T1_E3
 $R_{ds(ON)} = 22\text{ mohm}$ ($V_{gs} = 4.5V$)
 $I_{cont} = 6.5A$ ($T = 25^\circ C$)
 $I_{peak} = 40A$ (Pause $\geq 10\mu s$)
L-side MOSFET: SI7326DN_T1_E3
 $R_{ds(ON)} = 22\text{ mohm}$ ($V_{gs} = 4.5V$)
 $I_{cont} = 6.5A$ ($T = 25^\circ C$)
 $I_{peak} = 40A$ (Pause $\geq 10\mu s$)

Controller

- Voltage & Current:**
 $+12.6V @ 2.5A$
- Frequency:**
 $PR18 = 33KOHM, F_{osc} = 515KHz$
- OCV:**
N/A
- POR:**
 $POR\ Hysteresis = 0.1V$
 $V_{on} = 7.5V$
- Enable Voltage:**
 $V = 2.9V$
- Soft start time:**
 $T_{ss} = 23ms$
- Phase selection:**
N/A
- Inrush Current:**
 $C_{total} = 20\mu F$
 $I_{inrush} = 0.01A$

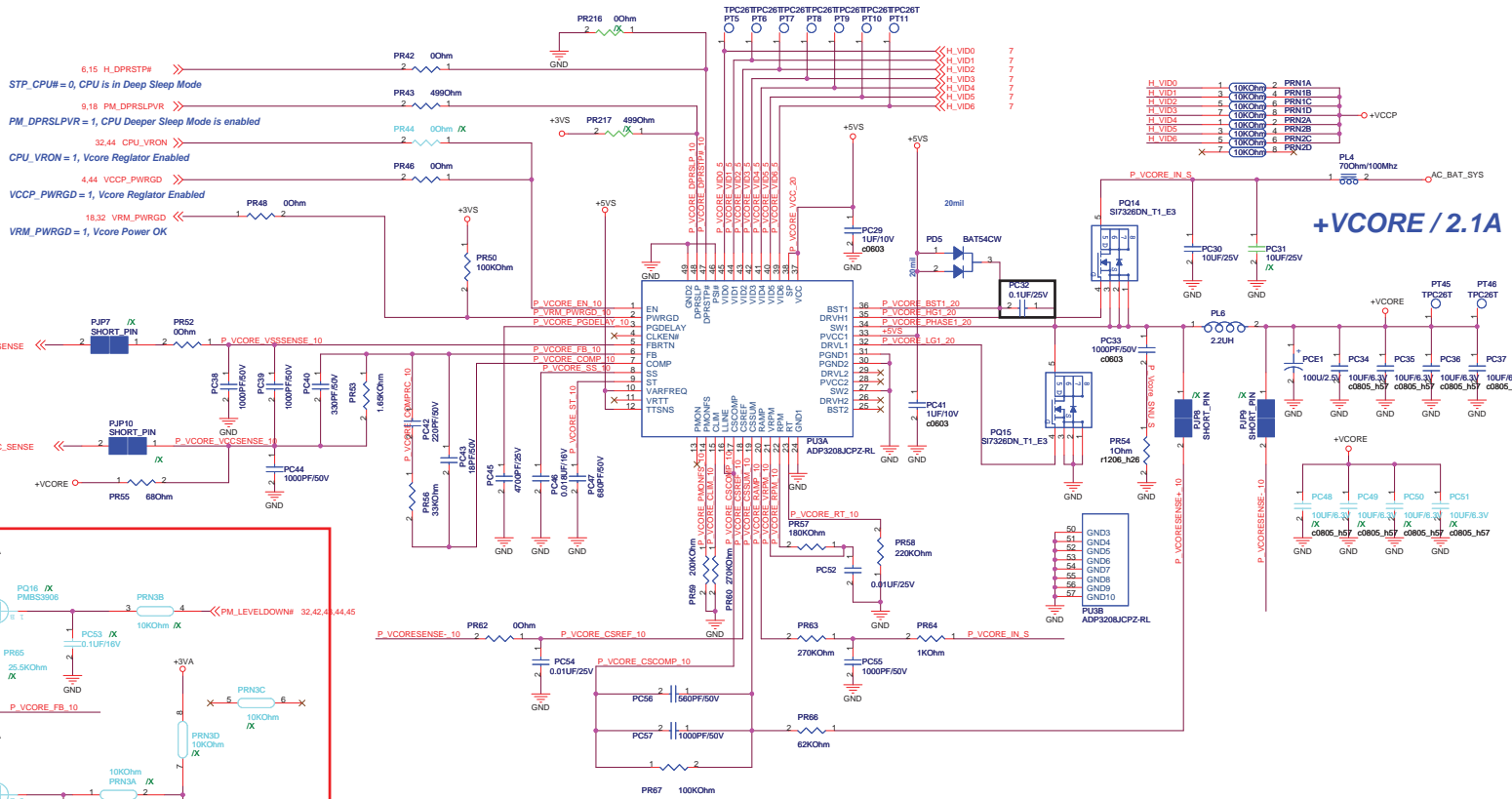


Battery Charging Current :
 $4.4V > V_{adj2} \geq 0V \Rightarrow$
 $I_{chg} = (V_{adj2} - 0.075) / (25 \cdot R_s)$
 $BATSEL_2P\# = 1, I_{ch} = 1.49A$
 $BATSEL_2P\# = 0, I_{ch} = 2.5A$
Input Adaptor Max. Current Limit :
 $I_{limit_current} = (V_{adj1} - 0.075) / (25 \cdot R_s) = 1.90A$

Pre-Charging Mode :
Precharging current = 149.2mA
 $V_{adj2} = 168mV$
ACIN Threshold = 1.25V
Adaptor > 13.75V, System Powered by Adaptor
Adaptor < 13.75V, System Powered by Battery

Battery Charging Voltage :
 $V_{adj3} : VREF \Rightarrow V_{bat} = 4.2V / cell$
 $3.9V > V_{adj3} > 2.4V \Rightarrow V_{bat} = 4.35V / cell$
 $V_{adj3} : GND \Rightarrow V_{bat} = 4.0V / cell$
 $2.2V > V_{adj3} > 1.1V \Rightarrow V_{bat} = 2 \cdot V_{adj3} / cell$
Battery Cell Selection :
CELLS: VREF \Rightarrow 4 Cells;
CELLS: OPEN \Rightarrow 3 Cells;
CELLS: GND \Rightarrow 2 Cells;

VREF = 5.0V
 $f_{osc}(KHz) = 17000 / RT (KOhm) = 515KHz$
Soft start: $t_s(s) = 0.13 \cdot CS (\mu F)$

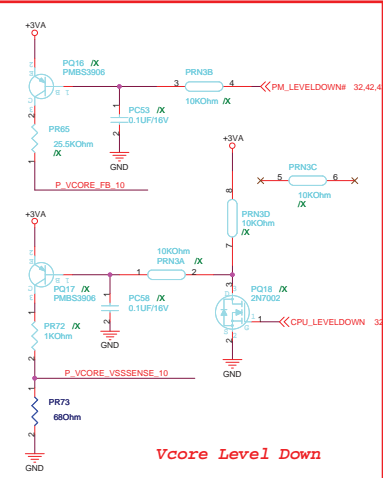


Power Stage

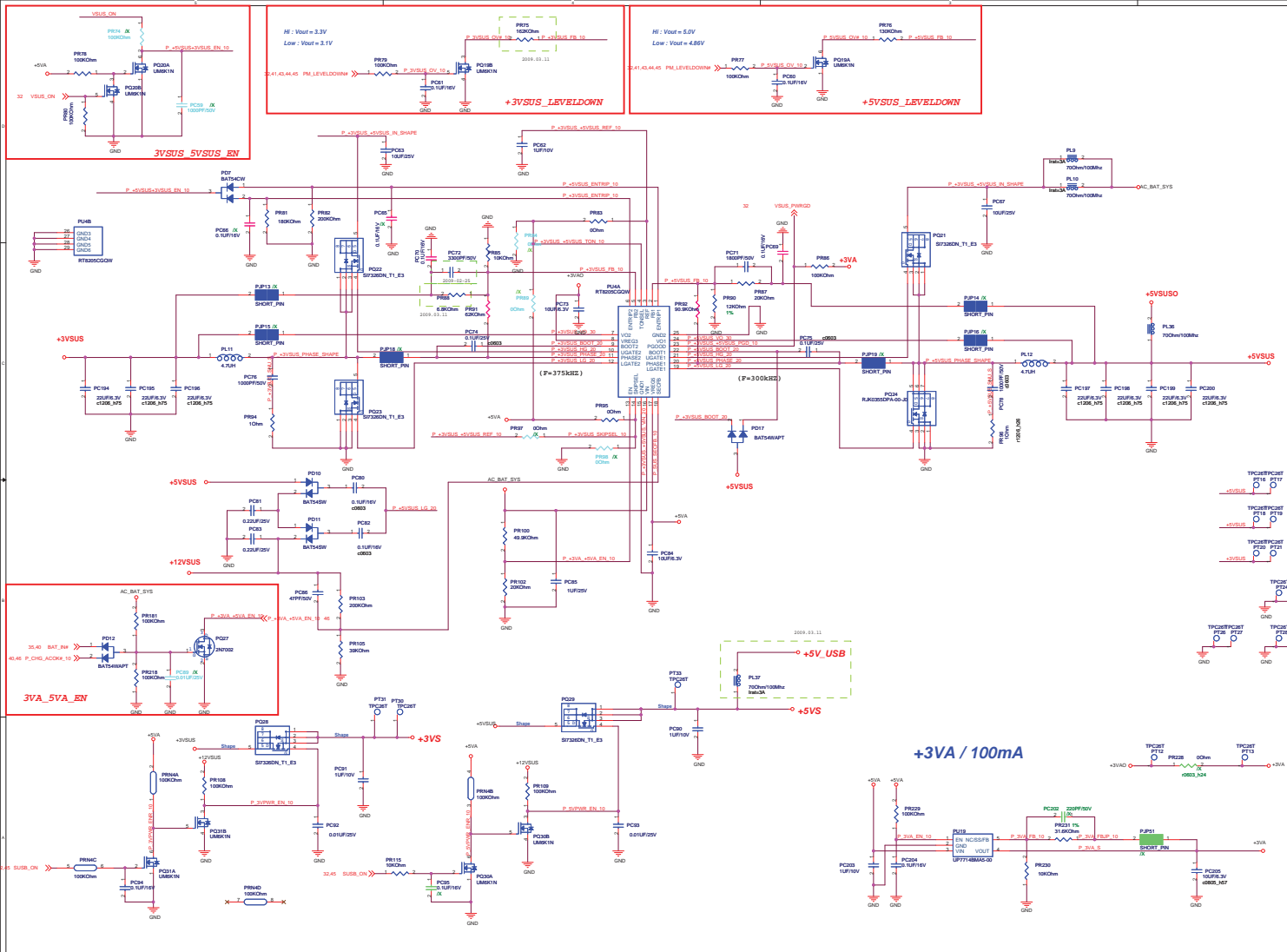
- I/P Current:**
 $I_{in} = V_o \cdot I_o / (0.8 \cdot V_{in}) = 0.32A$
- Ripple Current:**
 $I_{rip} = 0.6A$
 $I_{spec} = 2.5A$
- Dynamic:**
 $I_{peak} = 2.1A$
 $ESR / 1 \text{ pcs} = 18\text{mohm}$
 $V = 38\text{mV}$
- Inductor Spec:**
 $I_{sat} = 14A$
 $I_{dc} = 8A$
 $DCR = 18\text{mohm}$
- MOSFET Spec:**
H-side MOSFET: SI7326DN_T1_E3
 $R_{ds(ON)} = 22\text{mohm}$ ($V_{gs} = 4.5V$)
 $I_{cont} = 6.5A$ ($T = 25^\circ C$)
 $I_{peak} = 40A$ (Pause $\leq 10\mu s$)
L-side MOSFET: SI7326DN_T1_E3
 $R_{ds(ON)} = 22\text{mohm}$ ($V_{gs} = 4.5V$)
 $I_{cont} = 6.5A$ ($T = 25^\circ C$)
 $I_{peak} = 40A$ (Pause $\leq 10\mu s$)

Controller

- Voltage & Current:**
 $V_{CORE} = 0.5 - 1.5V @ 2.1A$
- Frequency:**
 $F_{osc} = 322\text{KHz}$ for RPM
 $F_{osc} = 272\text{KHz}$ for CCM
- OCP:**
 $I_{ocp} = 9.3A$
- POR:**
 $POR \text{ Hysteresis} = 0.15V$
 $V_{on} = 4.4 - 4.5V$
 $V_{off} = 4.0 - 4.2V$
- UVP:**
 $VID = 300mV$
- OVP:**
 $VID = 200mV$
- Soft start time:**
 $2.7ms$
- Phase selection:**
 $SP = VCC$
 single phase
- Loadline:**
 30mOhm



PM_LEVELDOWN#	CPU_LEVELDOWN	CPU_LEVELDOWN#	Vcore	Status
L	L	H	VID-150mV	Power Saving
H	L	H	VID	Normal
H	H	L	VID + 200mV	Performance
L	H	L	VID + 50mV	N/A



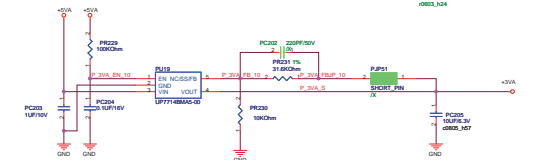
Power stage	+3VSUS
1. I/P Current:	$I_{in} = V_o/I_o / (0.8 * V_{in}) = 1.1A$
2. Ripple Current:	$I_{rip} = 1.36A$ $I_{spec} = 2.5A$
3. Dynamic:	$I_{peak} = 3A$ ESR / 1 pcs = 18 mohm $V = 54mV$
4. Inductor Spec:	$I_{sat} = 10 A$ $I_{dc} = 5.5 A$ DCR = 37 mohm
5. MOSFET Spec:	H-side MOSFET: SI7326DN_T1_E3 Rds(ON) = 22 mohm (Vgs = 4.5 V) I cont = 6.5 A (T = 25) I peak = 40 A (Pause ≥ 10 us)

Power stage	+5VSUS
1. I/P Current:	$I_{in} = V_o/I_o / (0.8 * V_{in}) = 1.67A$
2. Ripple Current:	$I_{rip} = 2.07A$ $I_{spec} = 2.5A$
3. Dynamic:	$I_{peak} = 3A$ ESR / 1 pcs = 18 mohm $V = 54mV$
4. Inductor Spec:	$I_{sat} = 10 A$ $I_{dc} = 5.5 A$ DCR = 37 mohm
5. MOSFET Spec:	H-side MOSFET: SI7326DN_T1_E3 Rds(ON) = 22 mohm (Vgs = 4.5 V) I cont = 6.5 A (T = 25) I peak = 40 A (Pause ≥ 10 us)

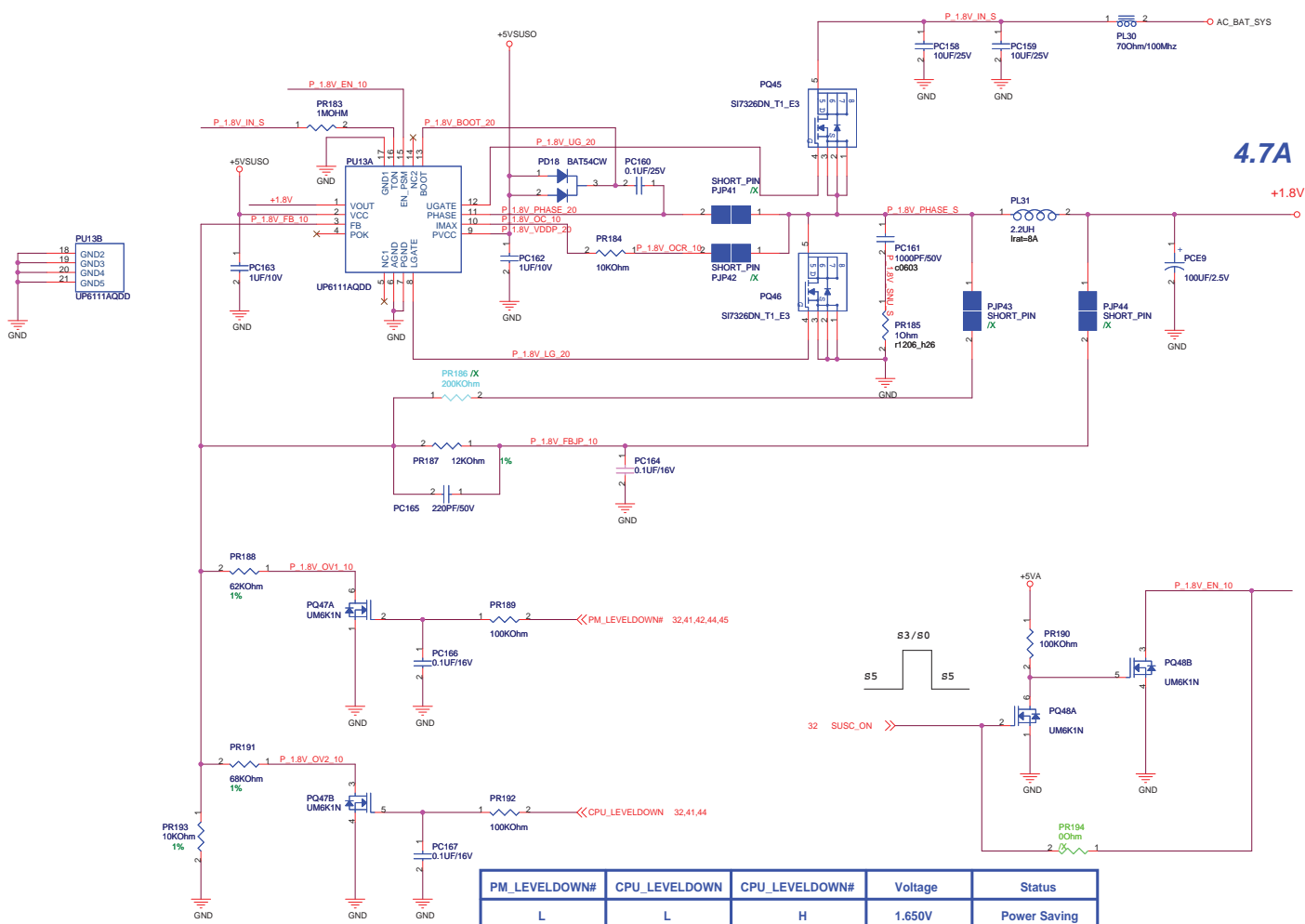
Controller	+3VSUS
1. Voltage & Current:	+3VSUS = 3.3V @ 3A
2. Frequency:	fosc = 375KHz
3. OCP:	Set PR1 = 180Kohm Iocp = 8A
4. POR:	V on = 4.35-4.5 V V off = 3.9-4.25 V
5. UVP:	V uvp = 70% Vout
6. OVP:	V ovp = 115% Vout
7. Enable Voltage:	V rising = 1V V falling = 0.4 V
8. Soft start time:	Tss = 2ms
9. Phase selection:	/X
10. Inrush Current:	C total = 100 uF I inrush = 0.165 A

Controller	+5VSUS
1. Voltage & Current:	+5VSUS = 5V @ 2.5A
2. Frequency:	fosc = 300KHz
3. OCP:	Set PR2 = 200Kohm Iocp = 17A
4. POR:	V on = 4.35-4.5 V V off = 3.9-4.25 V
5. UVP:	V uvp = 70% Vout
6. OVP:	V ovp = 115% Vout
7. Enable Voltage:	V rising = 1V V falling = 0.4 V
8. Soft start time:	Tss = 2ms
9. Phase selection:	/X
10. Inrush Current:	C total = 100 uF I inrush = 0.25 A

+3VA / 100mA



+3VA AEC / 100mA	
1. Dropout Voltage:	$V = 0.21V$ (Io = 0.3A)
2. OCP:	I ocp = 480mA
3. Short Circuit Current Limit:	I sc = 320mA
4. Power Dissipation:	Rthjc = 250 /W Pd = 0.4W
5. EN Voltage:	V en = 2V V sd =
6. Power OK Voltage:	Vpokth = 92% * Vout Vpokhys = 8%
7. Inrush current:	T ss = 400ns C total = 10uF I inrush =
8. Feedback Voltage:	VFB = 0.8 V



4.7A

Power stage

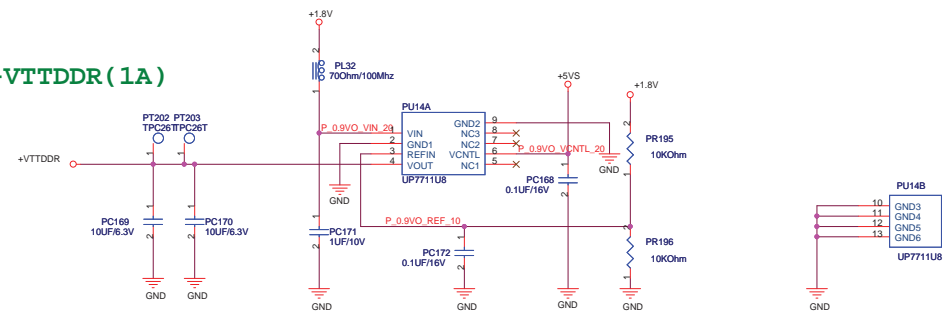
- I/P Current:**
 $I_{in} = V_o \cdot I_o / (0.8 \cdot V_{in}) = 1.175A$
- Ripple Current:**
 $I_{rip} = 1.88A$
 $I_{spec} = 2.5A \odot 1$
- Dynamic:**
 $I_{peak} = 4.7A$
 $ESR / 1\text{ pcs} = 18\text{ mohm}$
 $V = 84.6mV$
- Inductor Spec:**
 $I_{sat} = 14A$
 $I_{dc} = 8A$
 $DCR = 18\text{ mohm}$
- MOSFET Spec:**
H-side MOSFET: SI7326DN_T1_E3
 $R_{ds(ON)} = 22\text{ mohm}$ ($V_{gs} = 4.5V$)
 $I_{cont} = 6.5A$ ($T = 25^\circ C$)
 $I_{peak} = 40A$ (Pause $\geq 10\text{ us}$)
L-side MOSFET: SI7326DN_T1_E3
 $R_{ds(ON)} = 22\text{ mohm}$ ($V_{gs} = 4.5V$)
 $I_{cont} = 6.5A$ ($T = 25^\circ C$)
 $I_{peak} = 40A$ (Pause $\geq 10\text{ us}$)

Controller

- Voltage & Current:**
+1.8V @ 5.8A
- Frequency:**
 $PR183 = 1M\text{ ohm}$
 $F_{osc} = 250KHz$
- OCP:**
 $PR184 = 10K\text{ ohm} \rightarrow 9A$
- POR:**
 $V_{ccrth} = 3.7\text{--}4.1V$
 $V_{cchys} = 0.2V$
- UVP:**
 $V_{out} = 70\%$
- OVP:**
 $V_{out} = 115\%$
- Enable Voltage:**
 $V = 2.9V$
- Soft start time:**
 $T_{ss} = 1.2\text{ ms}$
- Phase selection:**
 $/X$
- Inrush Current:**
 $C_{total} = 100\text{ uF}$
 $I_{inrush} = 0.15A$

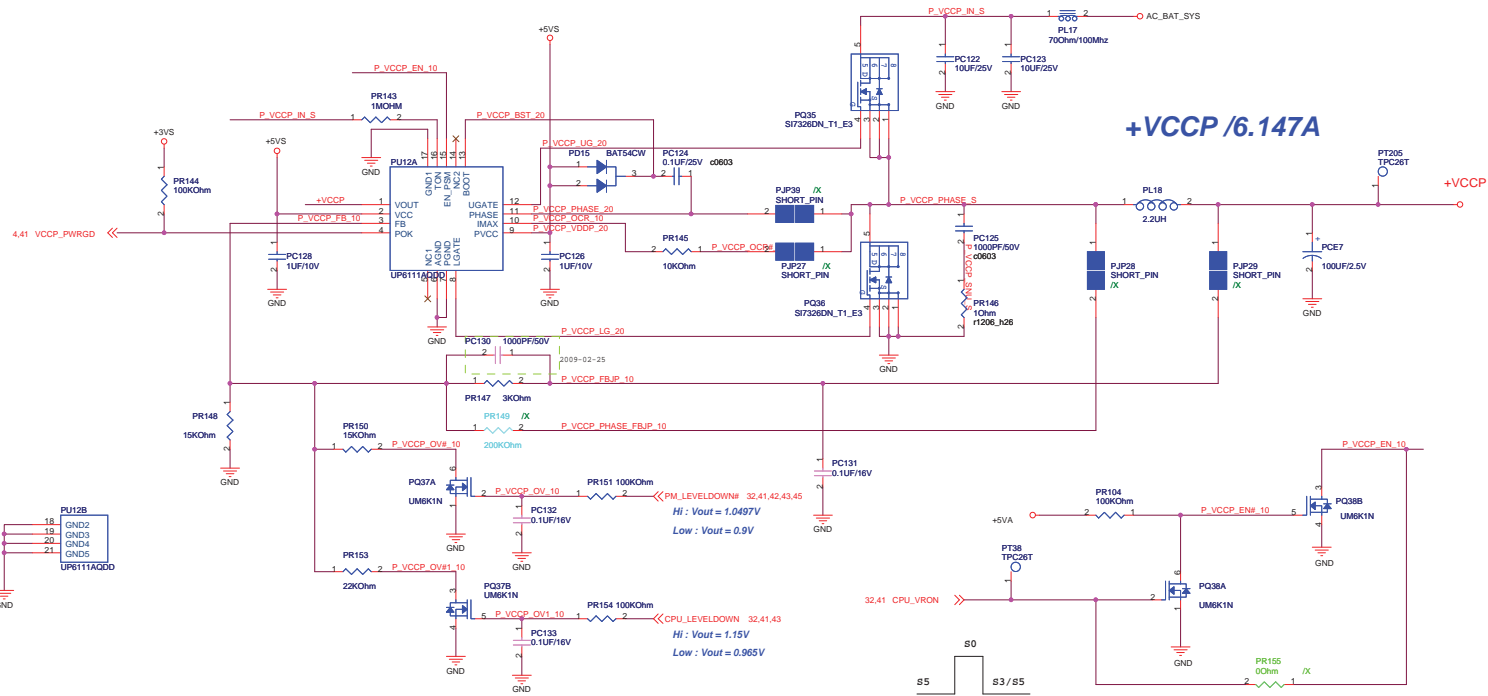
PM_LEVELDOWN#	CPU_LEVELDOWN	CPU_LEVELDOWN#	Voltage	Status
L	L	H	1.650V	Power Saving
H	L	H	1.795V	Normal
H	H	L	1.927V	Performance
L	H	L	1.782V	N/A

+VTDDR (1A)



+VTDDR@1A

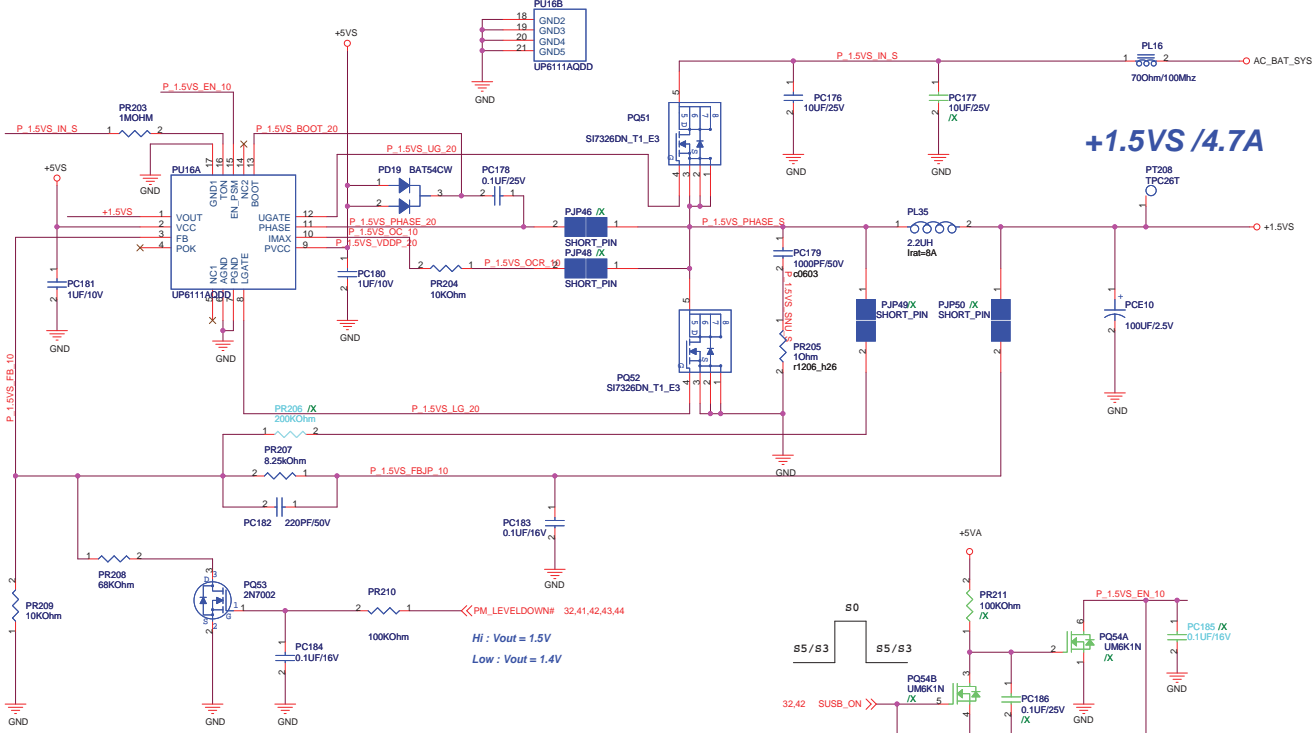
- Dropout Voltage:**
 $V = 0.3V$ ($I_o = 2A$)
- Current Limit:**
 $I_{limit} = 4A$
- Continue Current:**
 $I_{cont} = 3A$
- Power Dissipation:**
 $R_{thjc} = 52 /W$
 $P_d = 1.9W$
- EN Voltage:**
 $V_{en} = 1.4V$
 $V_{sd} = 0.8V$
- Supply Voltage:**
 $V_{cc} = 5V$
- Inrush current:**
 $T_{ss} = 5\text{ ms}$
 $C_{total} = 10\text{ uF}$
 $I_{inrush} = 1.8\text{ mA}$



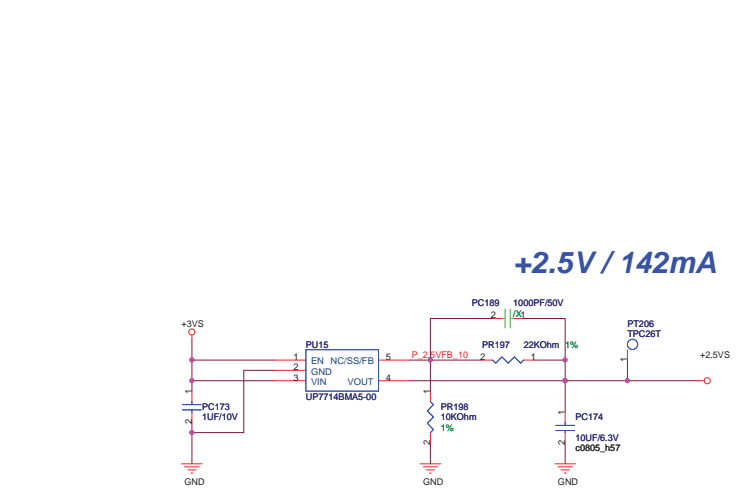
- ### Power stage
- I/P Current:**
 $I_{in} = V_o \cdot I_o / (0.8 \cdot V_{in}) = 0.89A$
 - Ripple Current:**
 $I_{rip} = 1.93A$
 $I_{spec} = 2.5A \odot 1$
 - Dynamic:**
 $I_{peak} = 6.147 A$
 $ESR / 1 \text{ pcs} = 18 \text{ mohm}$
 $V = 110mV$
 - Inductor Spec:**
 $I_{sat} = 14 A$
 $I_{dc} = 8 A$
 $DCR = 18 \text{ mohm}$
 - MOSFET Spec:**
H-side MOSFET: SI7326DN_T1_E3
 $R_{ds(ON)} = 22 \text{ mohm}$ ($V_{gs} = 4.5 V$)
 $I_{cont} = 6.5 A$ ($T = 25^\circ C$)
 $I_{peak} = 40 A$ (Pause $\geq 10 \mu s$)
L-side MOSFET: SI7326DN_T1_E3
 $R_{ds(ON)} = 22 \text{ mohm}$ ($V_{gs} = 4.5 V$)
 $I_{cont} = 6.5 A$ ($T = 25^\circ C$)
 $I_{peak} = 40 A$ (Pause $\geq 10 \mu s$)

- ### Controller
- Voltage & Current:**
+VCCP@6.147A
 - Frequency:**
 $PR143 = 1.3M \text{ ohm}$
 $F_{osc} = 188KHz$
 - OCP:**
 $PR145 = 10K \text{ ohm} \rightarrow 9A$
 - POR:**
 $V_{ccrth} = 3.7 \sim 4.1V$
 $V_{cchys} = 0.2V$
 - UVP:**
 $V_{out} * 70\%$
 - OVP:**
 $V_{out} * 115\%$
 - Enable Voltage:**
 $V = 2.9V$
 - Soft start time:**
 $T_{ss} = 1.2 \text{ ms}$
 - Phase selection:**
 $/X$
 - Inrush Current:**
 $C_{total} = 100 \mu F$
 $I_{inrush} = 0.0875 A$

PM_LEVELDOWN#	CPU_LEVELDOWN	CPU_LEVELDOWN#	Voltage	Status
L	L	H	0.9V	Power Saving
H	L	H	1.050V	Normal
H	H	L	1.152V	Performance
L	H	L	1.002V	N/A



+1.5VS /4.7A



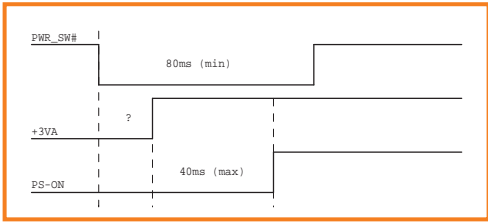
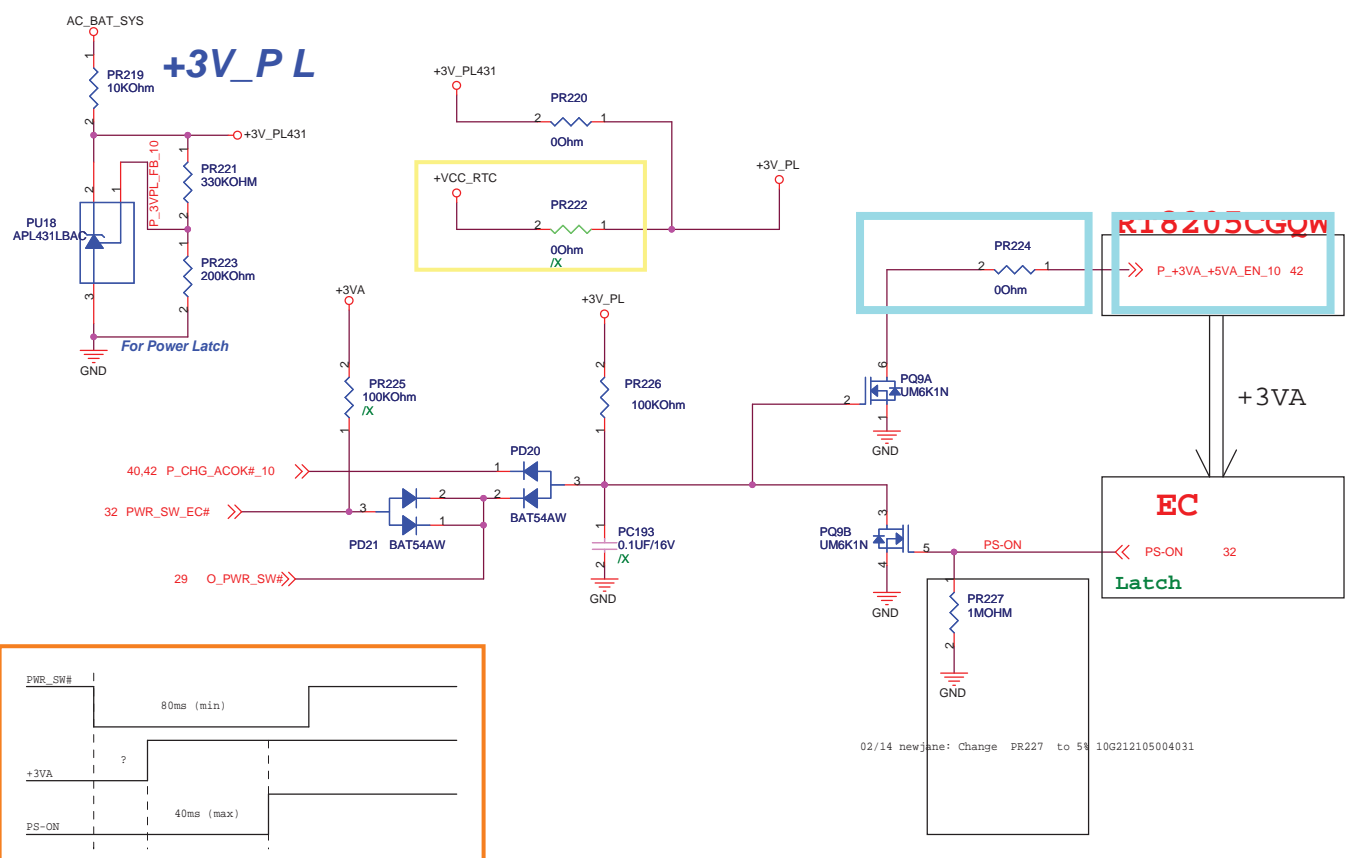
+2.5V / 142mA

Power stage

- I/P Current:**
 $I_{in} = V_o * I_o / (0.8 * V_{in}) = 0.83A$
- Ripple Current:**
 $I_{rip} = 1.5A$
 $I_{spec} = 2.5A @ 100\mu s$
- Dynamic:**
 $I_{peak} = 4.7A$
 $ESR / 1\text{ pcs} = 18\text{ mohm}$
 $V = 84.6mV$
- Inductor Spec:**
 $I_{sat} = 14A$
 $I_{dc} = 8A$
 $DCR = 18\text{ mohm}$
- MOSFET Spec:**
H-side MOSFET: SI7326DN_T1_E3
 $R_{ds(ON)} = 22\text{ mohm}$ ($V_{gs} = 4.5V$)
 $I_{cont} = 6.5A$ ($T = 25^\circ C$)
 $I_{peak} = 40A$ (Pause $\geq 10\mu s$)
L-side MOSFET: SI7326DN_T1_E3
 $R_{ds(ON)} = 22\text{ mohm}$ ($V_{gs} = 4.5V$)
 $I_{cont} = 6.5A$ ($T = 25^\circ C$)
 $I_{peak} = 40A$ (Pause $\geq 10\mu s$)

Controller

- | | |
|---|---|
| <ol style="list-style-type: none"> Voltage & Current:
+1.5VS @ 4.7A Frequency:
$PR203 = 1M\text{ ohm}$
$F_{osc} = 250KHz$ OCP:
$PR204 = 10K\text{ ohm} \rightarrow 9A$ POR:
$V_{ccrth} = 3.7\sim 4.1V$
$V_{ccchys} = 0.2V$ UVP:
$V_{out} = 70\%$ | <ol style="list-style-type: none"> OVP:
$V_{out} * 115\%$ Enable Voltage:
$V = 2.9V$ Soft start time:
$T_{ss} = 1.2\text{ ms}$ Phase selection:
$/X$ Inrush Current:
$C_{total} = 100\mu F$
$I_{inrush} = 0.125A$ |
|---|---|



Title	<Title>	
Size	Document Number	Rev
A3	<Doc>	<RevCode>
Date:	Thursday, March 19, 2009	Sheet 46 of 48

Ver	Description	Date
1.0G	change UF1 to the same as 1005hn's	2009.0122.2027
	change lvds conn P/N to 12G170190201 change CPU P/N from 01G012290000 to 01G012520100 P4: 糞 CC50 ..CC57 監茶臂 clock gen pin 狼 P23: 糞 GC21 P29: 奔IL2	2009.0203.1555
	update NB symbol 癸clock gen cm WIFI 场だ 酚1005HN 和≡ 穢	2009.0205.1555
	P4: C_PCIE_LAN_R C_PCIE_LAN#_R H_ITP_CKOUT H_ITP_CKOUT# add 10pf for RF P23: cancel BL_EN, G_LVDD_EN, G_NBL_CTRL EMI cap	2009.0205.2120
	ADD LR55 02/14 newjane: Change PR227 to 5% 10G212105004031 02/14 newjane: Change OR1 from 18.2K to 18K 10G212180214010 02/14 newjane: Change HR1 from 68ohm to 56 ohm 02/14 newjane: Change SR1 from 20K 10G212200214110 to 20K 10G212200214030 02/14 newjane: ChangeHC18 from 11G23211021115 to 11G232110214030 02/14 newjane: ChangeHC6 GC20 HC11 HC12 from 11G233310531360 to 11G233210516320 02/14 newjane: /X LC41 02/14 newjane: SD RC1 RC7 RC12 from 11G232310431360 to 11G232110411320 02/14 xiao-jie SR4 PR227 from 10G212105004031 to 10G212100414030 02/14 xiao-jie aAR8 AR5 from 10G212200214110 to 10G212200214030 02/14 xiao-jie AR7 P/N to PR105 P/N	2009.0210.1513

		Title : <Title>	
<OrgName>		Engineer: Lus Lu	
Size A3	Project Name <Doc>	Rev 1.0	
Date: Thursday, March 19, 2009		Sheet 47 of 48	

